Modular Computers ®

VMP1

Power PC-based CPU Board for VME Applications

Manual ID 19972, Rev. Index 0101
Apr 00

CE

The product described in this manual is in compliance with all applied CE standards.

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Revision History

Revision History			
Manual/Product Title:	**VMP1**		
Manual ID Number:	**19972**		
Rev. Index	**Brief Description of Changes**	**Board Index**	**Date of Issue**
0100	Initial Issue	01	Mar. 00
0101	Correction to Table 4-1, page 4-3	01	Apr. 00

Trademarks

Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please see also the section “Applied Standards” in this manual.

Caution!

This symbol and title warn you of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the necessary precautions as described and/or prescribed by the law may result in damage to your product and/or endanger your life/health.

Please see also the section “High Voltage Safety Instructions”.

ESD-Sensitive Device!

This symbol and title highlight the fact that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following pageof this manual.

Attention!

This symbol and title emphasize aspects which, if not understood and taken into consideration by the reader, may result in hazards to health and/or material damage.

Note:

This symbol and title relate to information the user should read through carefully for his or her own advantage.

PEP Advantage

This symbol and title accompany information highlighting positive aspects of a *PEP* product and/or procedure.

Troubleshooting

This symbol and title accompany information about troubleshooting and problem solving.

For your safety

Your new *PEP* product has been developed and carefully tested in order to provide all the features necessary to ensure full compliance with all electrical safety requirements. It has also been designed for a long fault-free life. However, the life expectancy of your product will be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interests of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel.

Caution!

The power supply must always be disconnected before installation, repair and maintenance operations are carried out on this product. Failure to comply with this basic precaution will subject the operator to serious electrical shock hazards. Always unplug the power cable before such operations.
Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Care must therefore be exercised at all times during handling and inspection of the board, in order to ensure product integrity.

- Do not handle this product while it is outside its protective enclosure while it is not used for operational purposes, unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where safe work stations are not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instructions on the previous page of this manual.

Two Year Warranty

PEP Modular Computers grants the original purchaser of a *PEP* product a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of *PEP* are valid unless the customer has the express written consent of *PEP Modular Computers*.

PEP Modular Computers warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than *PEP Modular Computers* or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided he should, in the event of any claim, return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application in which the product has been used and a description of the defect. Please pack the product in such a way as to ensure safe transportation (see our safety instructions).

PEP provides for repair or replacement of any part, assembly or sub-assembly at the company's own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to *PEP Modular Computers*, and the remaining portion of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by *PEP* with the repaired or replaced item.

PEP Modular Computers will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refund. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of *PEP Modular Computers* liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

PEP Modular Computers issues no warranty or representation, either explicit or implicit, with respect to its products' reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will *PEP* be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if *PEP* were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no *PEP Modular Computers* employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's prior consent.

Chapter 1

Introduction

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1. Introduction

The VMP1 is a comprehensive computing platform which brings togethor the latest advances in computing technology in a board designed for maximum performance, flexibility and versatility within a rugged compact format.

The design centered on realizing a board which addresses the need for increased computing capacity while at the same time reducing the size and number of system components in order to reduce space requirements and optimize power dissipation.

The VMP1 is based on the MPC8240, a highly integrated microprocessor containing a PowerPC MPC603e core. This is the 250 MHz version with a Floating Point Unit (FPU). One of the prime advantages of utilizing the established and proven MPC603e core is the associated broad infrastructure of support that has built up around it . All of the noteworthy third-party software tool vendors provide tools for the MPC8240.

An important feature of the board is the integration of a PCI bus within a VME-CPU board. This connects the MPC8240 with the Fast Ethernet controller and the Tundra Universe II PCI/VME bridge and also to the onboard 100-pin PCI expansion connector, enabling the connection of the full range of PCI peripherals.

The VMP1 employs an OS-independent boot loader that enables the loading of any operating system. This boot loader makes an update of the Flash contents and automatically downloads from Flash to SDRAM before booting the OS. For performance reasons the OS is started from the SDRAM.

The power of the board is greatly enhanced by means of the PCI expansion connector which makes it possible to cascade one or two additional IO1 modules onto the board resulting in a total package of either 8HP or 12HP. Both IO1 modules may be used to carry PMC modules. Given the wide range of PMC modules now available, this feature affords the user a very wide range of options. Additionally, one can substitute a module designed to provide an even greater range of PCI peripherals in place of either of the IO1 modules. These features enable, for example, the connection of the widest range of system I/O components such as various field busses, Fast Ethernet and Ultra 2 SCSI, to name just a few. The complete range of expansion possibilities is thus made available to the user by the VMP1.

1.1 Board Introduction

The VMP1 is a VME PowerPC-based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the VMP1's outstanding features are:

- PowerPC MPC8240 Kahlua (603E core with an integrated FPU, combined with PCI interface and memory controller)
- 16 kB data cache
- 16 kB instruction cache
- up to 128 MB SDRAM (100MHz) with optional ECC support
- up to 8 MB onboard Flash
- Fast Ethernet interface
- two serial I/O's (RS232 / ESD protected and EMI compliant)
- Memory Expansion Socket e.g. Flash memory (up to 144 MB) or SRAM
- onboard PCI bus with expansion connector
- four counter/timers
- programmable watchdog timer
- real-time clock
- double-width version for PCI expansion
- Tundra Universe II VME-to-PCI Bridge
- compliance with VITA VME-Specification ANSI / IEEE STD1014-1987 / IEC 821 and 297

1.2 Board Overview

The VMP1 is a 3U VME CPU board featuring a powerful CPU (number cruncher). The design is based on the new highly integrated Motorola PowerPC processor MPC8240, which integrates a PCI interface and several peripherals inside one Chip.

Two standard memory configurations (32 MB or 64 MB SDRAM) are available, with 128 MB available on request. Flash memory for integrating the initial bootloader and ROMable operating systems are provided . Additionally, NV SRAM or a Disk-On-Chip (by M-Systems) can be placed on a DIL socket for special purposes.

The board controls the VMEbus through the Tundra UNIVERSE II PCI-VME bridge which is an industrial standard for connecting the PCI bus to the VME. Improved VMEbus master and VMEbus slave performance with an increase of FIFO depth and optimized DMA transfer are some of the outstanding features of this device.

The VMP1 is also able to communicate with the environment through a Fast Ethernet interface and two serial interfaces at the front side of the board. One of the serial interfaces is a RS232 full modem interface while the other is a software-configurable RS232/RS485 port. These UARTS support baud rates up to 1.5 Mbps and are software compatible with the 16550 UART from National Semiconductor. They contain 128 Byte Transmit FIFO and 128 Byte Receive FIFO for reducing the bandwidth requirement of the CPU.

The Ethernet is realized with the Intel 82559 with full duplex support at both 10/100 Mbps possible. This Fast Ethernet controller with an integrated 10/100 Mbps physical layer device is the foremost solution for PCI board LAN designs. It combines low power consumption with a small package design which is ideal for power and space constrained environments.

Anticipating the VMP1's use in data critical applications, the memory data path contains a selectable in-line ECC controller which can provide SDRAM single-bit error correct or double-bit error detect.

For mass data transmission a dual channel DMA controller is provided. It can be programmed directly or through the use of descriptor chains located in memory. Data can thus be moved from PCI to memory or vice versa, memory to memory, or PCI to PCI.

The MPC8240 supports processor control and visibility through the JTAG/COP (common on-chip processor) interface that is available on the VMP1. Utilizing third party tools, the developer can access and control the processor. It also has standard IEEE 1149.1a-1993 compliant boundary scan capability. The ECC data path has a mechanism to manually inject errors into memory for use with maintenance and diagnostic utilities. Furthermore a watch point and capture register on the internal bus and a set of address attributes on the external memory and PCI buses facilitate debugging analysis.

VME interface

In addition to the standard functionality required by a VME CPU, the VMEbus interface (Tundra Universe 2) provides:

- automatic First-Slot detection
- integral FIFO buffers for multiple transactions in both directions
- programmable DMA controller with linked list support.
- Mailbox

1.3 VMP1 Main Specifications

Table 1-1: VMP1 Main Specifications

VMP1	Specifications
Operating System Support	Initial boot loader with capability to load VxWorks and other Real-time operating systems
VME Interface	ANSI/VITA 1-1994 for VME, approved April 10, 1995 Support for A24: D16/D8 master and A24: D16/D8 slave interface
Processor	Motorola MPC8240 with integrated PCI interface 250MHz
Boot Device	8 MB Flash for bootloader and ROMable OS / Socket
Main Memory	32 MB or 64 MB of onboard SDRAM with ECC support available as standard (128 MB available on request)
Cache Structure	16K, 32 byte line, 4-way set associative instruction cache 16K, 32 byte line, 4-way set associative data cache
Flash	8 MB on-board Flash (soldered)
DIL600 Socket	Socket for Flash extension by another 512 kB or addition of Flash disk (M-System) with up to 144 MB
PCI Expansion Connector	1 x Samtec SMT Board-to-Board connector 100-pin order number: FLE - 15 - 01 - G - DV
Ethernet	10Base-T / 100Base-TX
SRAM	256 or 512 kB NV SRAM on the DIL600 socket
Serial Port	16550 compatible Dual UART; 2 x RS-232 or 1 x RS232 + 1 x RS485
Watchdog	Watchdog generates Exception Condition / Reset or NMI (software configurable)
RTC	backed up with GoldCap / Data retention for about 5 days / backup battery possible
EEPROM	1 x 24LC16 for special purposes (8x256Byte)
LED's	6 LED's: red = general purpose yellow = watchdog active green = general purpose green = Ethernet Link Integrity, green = Ethernet Activity green = Ethernet Speed
Switches	Two push-buttons (Reset and Abort)

Table 1-1: VMP1 Main Specifications

VMP1	Specifications
Debug Interface	JTAG/BDM
VME Connector	96-pin VME connector
Onboard Connectors	2 x RJ45 for RS232, 1 x RJ45 for Ethernet
PCI Expansion Modules	PMC carrier, future PCI based I/O board with VGA/SCSI/2nd Ethernet
Mechanical Conformance	Conforms with IEEE 1101.10
Power Supply	5V in accordance with the VME Specification, 1.79 Amp current
Temperature Range	–40°C to +85°C (operating) –55°C to +125°C (storage)
Humidity	0% to 95% non-condensing
Dimensions	100mm x 160mm single-height Eurocard
Board Weight	182 grams

1.4 Applied Standards

1.4.1 CE Compliance

The *PEP Modular Computers'* VME systems comply with the requirements of the following CE-relevant standards:

- Emission EN50081-1
- Immission EN50082-2
- Electrical Safety EN60950

1.4.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.10

1.4.3 Environmental Tests

- Vibration IEC68-2-6
  Random Vibration, Broadband IEC68-2-64 (3U boards)
- Permanent Shock IEC68-2-29
- Single Shock IEC68-2-27

1.5 Related Publications

1.5.1 VME Systems/Boards

VME Specification, ANSI/VITA 1-1994 for VME, approved April 10, 1995

1.5.2 PMC Add-on Modules/Carriers

- Draft Standard for a Common Mezzanine Card Family, P1386/Draft 2.0
- Draft Standard Physical and Environment Layers for PCI Mezzanine Cards, P1386.1/Draft 2.0

Chapter 2

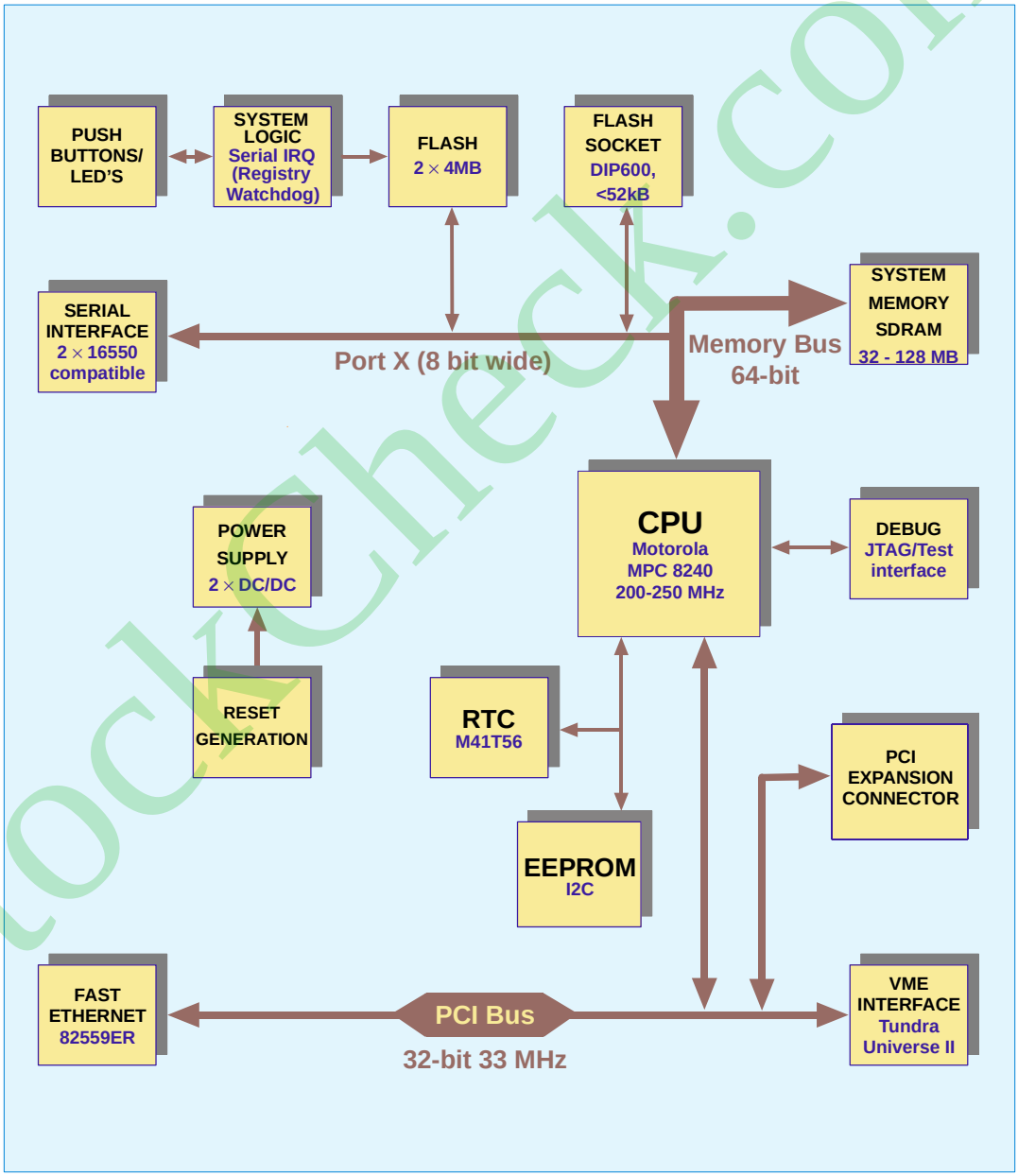
Functional Description

Functional Description

2. Functional Description

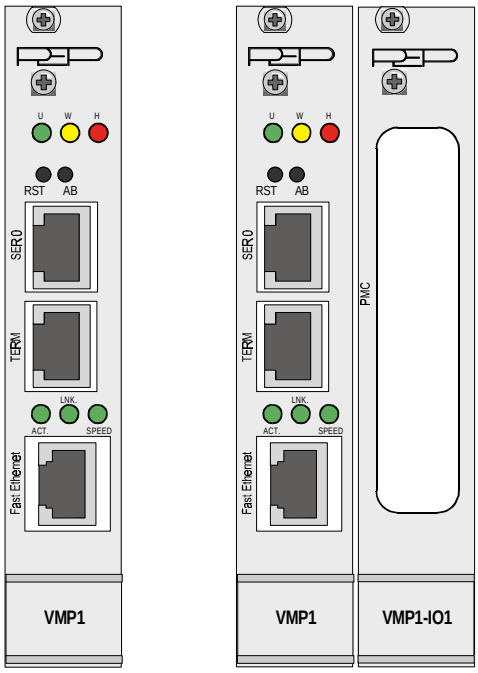
2.1 Functional Block Diagram

Figure 2-1: Functional Block Diagram



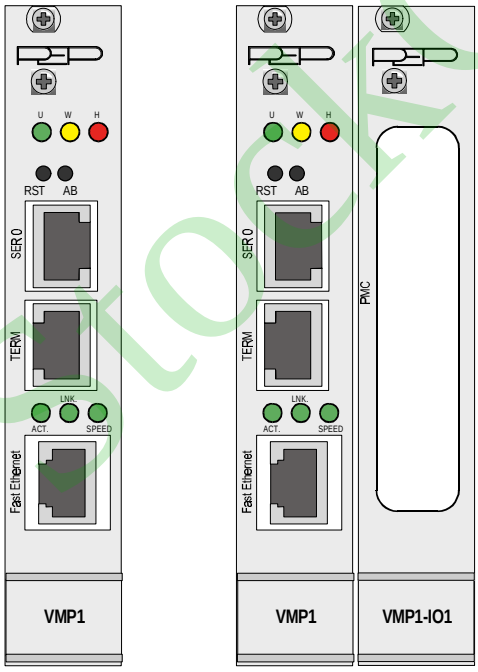
2.2 Front Panels

Figure 2-2: Front Panels



Standard VMP1 and Standard with IO1 Module

KEY
LED colors (for B&W monitors and printouts):
U = green
W = yellow
H = red



VMP1 Optoisolated version and Optoisolated version with IO1 Module - note the different position of the SER 0 connector

2.3 Board Layout

Figure 2-3: VMP1 Board (Front View)

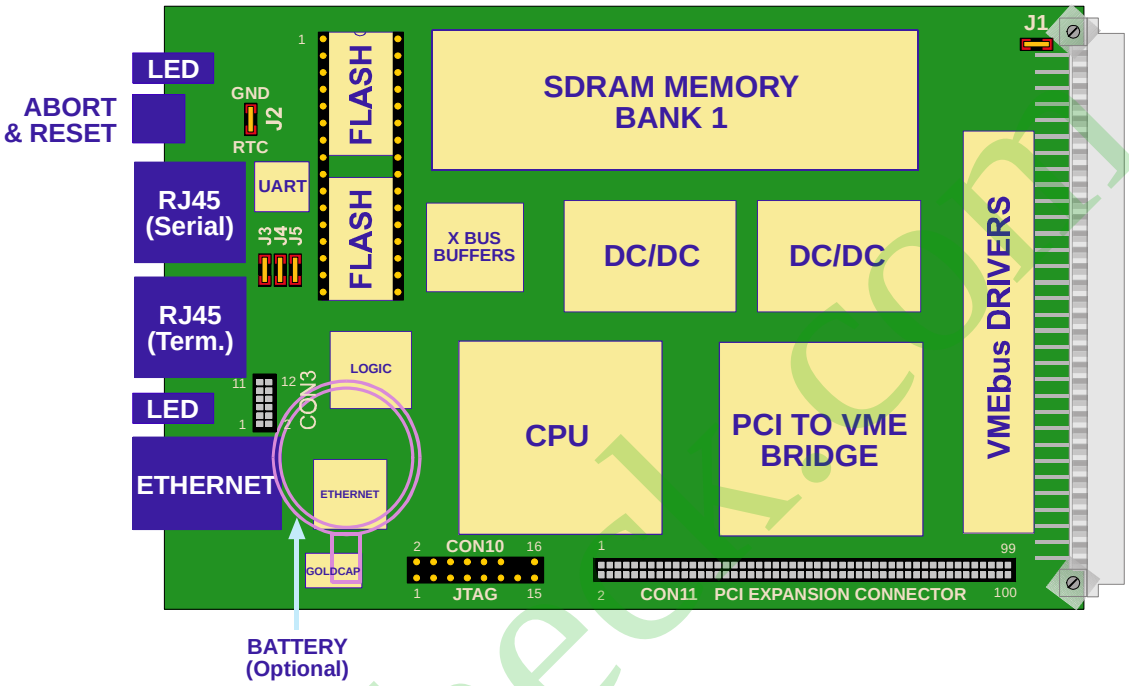
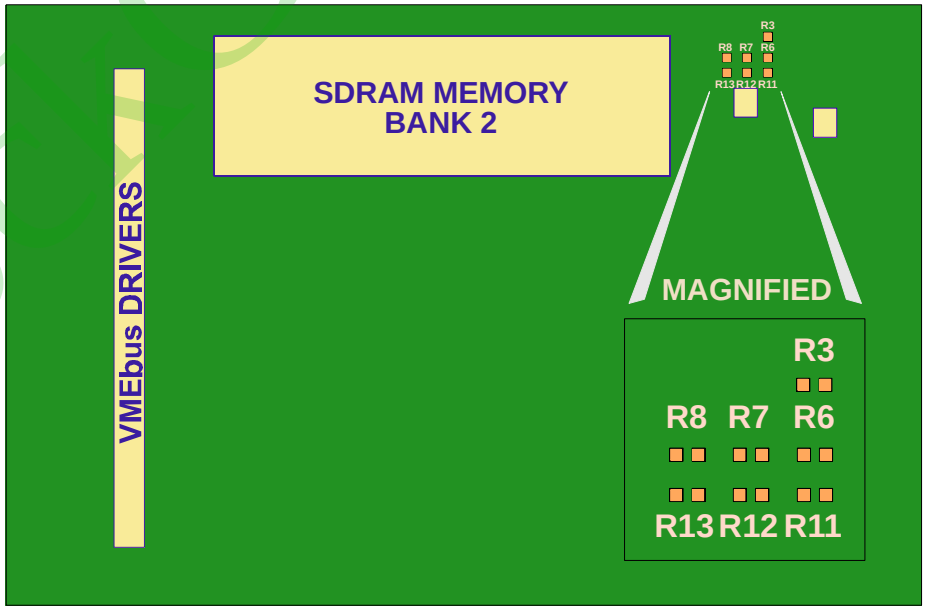


Figure 2-4: VMP1 Board (Reverse View)



2.4 Main Features

The following descriptions provide an overview of the main features of the principal functional blocks of the VMP1.

2.4.1 CPU

The VMP1 is based on the Motorola PowerPC processor MPC8240 which integrates a large number of peripherals, such as a PCI interface, PCI arbiter, Interrupt Controller, Memory Controller and multiple Timers. CPU speed is 250 MHz.

2.4.1.1 MPC8240 (Kahlua) Features

Important features of the MPC8240 implemented on the VMP1 are as follows:

Peripheral logic

Memory interface

- Programmable timing supporting either FPM DRAM, EDO DRAM or SDRAM (The VMP1 uses SDRAM at 100 MHz)
- High bandwidth bus (64-bit data bus) to SDRAM
- 2 memory banks with up to 64 MB each (64 or 128 Mbit memory devices)
- Supports 32, 64, 96 and 128 MB SDRAM
- Contiguous memory mapping
- 8-bit ROM interface
- Write buffering for PCI and processor accesses
- Supports ECC
- SDRAM data path buffer
- Low voltage transistor-to-transistor logic (LVTTL)
- Port X: 8-bit general-purpose I/O port using ROM controller interface with address strobe

32-bit PCI interface operating up to 33 MHz on the VMP1

- PCI Specification Revision 2.1 compatible
- PCI 5.0-V tolerance
- Support for PCI-locked accesses to memory
- Support for accesses to all PCI address spaces
- Selectable big- or little-endian operation
- Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- Memory prefetching of PCI read accesses
- Selectable hardware-enforced coherency
- PCI bus arbitration unit (five request/grant pairs)

PCI agent mode capability

- Address translation unit
- Internal configuration registers accessible from PCI
- Two-channel integrated DMA controller
- Supports direct mode or chaining mode (automatic linking of DMA transfers)
- Supports scatter gathering - read or write discontinuous memory
- Interrupt on completed segment, chain, and error
- Local-to-local memory
- PCI-to-PCI memory
- PCI-to-local memory
- Local-to-PCI memory

Message unit

- I2O message controller
- Two door-bell registers
- In-bound and out-bound messaging registers

I2C controller with full master/slave support

Embedded programmable interrupt controller (EPIC)

- Five hardware interrupts (IRQs) or 16 serial interrupts
- Four programmable timers

Integrated PCI bus and SDRAM clock generation

Programmable memory and PCI bus output drivers

Debug features

- Watchpoint monitor
- Address attribute and PCI attribute signals
- JTAG/COP - common onboard processor for in-circuit hardware debugging
- Performance monitor

603e core

High performance, superscalar 603e core

SPECint95 = 6.2 / SPECfp95 = 5.2 / 352Dhrystone (2.1) MIPS

Integer unit (IU), floating point unit (FPU) (user enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)

16 kB instruction cache

16 kB data cache

Lockable L1 cache - entire cache or on a per-way basis

Dynamic power management

2.4.2 Memory

2.4.2.1 System Memory (DRAM)

The main memory of the VMP1 consists of 32 MB or 64 MB SDRAM (128 MB available on request) soldered onto the board for mechanical stability.

The VMP1 provides ECC support (optional) and a maximum memory speed of 100MHz.

2.4.2.2 Flash

4 or 8 MB of soldered Flash memory accommodate the bootstrap loader software and can be used to store ROMable operating systems or user data. This Flash memory is 8-bit wide and windowed with window sizes of 512 kB.

2.4.2.3 EEPROM

A serial EEPROM is provided, organised into 8 blocks with 256 bytes per block (24LC16). This EEPROM is connected to the I2C bus provided by the MPC8240.

2.4.2.4 Memory Expansion Socket (DIL600)

The VMP1 provides one 32-pin DIL socket on which to place SRAM, non-volatile SRAM or other DIL600 devices on the board. Access to this Memory is controlled by the onboard logic.

The following devices may be added to the VMP1 via the 32-pin DIL600 socket:

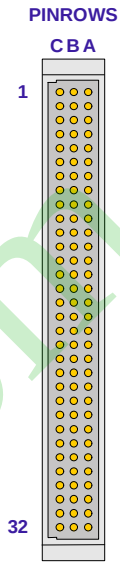
- Standard Flash memory of up to 512 kB, for example, the AMD29F010 and AMD29F040
- The NV SRAM from Dallas Semiconductor. These devices are available in the temperature range –40°C to +85°C for the industrial environment and guarantee a minimum data retention of 10 years (e.g. DS1250Y-100).
- Disk-on-chip Flash memory. In order to achieve flexibility with low cost, the VMP1 Flash disk is not soldered but connected via a special module from M-Systems (Disk-on-Chip 2000) which comes in the following sizes:

  2 - 24 MB (dimensions 41.7 x 17.9 x 5.6mm);

  4 - 144 MB (dimensions 42.0 x 18.3 x 11.8mm).

2.4.3 Board Interfaces

2.4.3.1 VME Interface and Pinout



The VME interface is based on the TUNDRA UNIVERSE II Bridge, which includes the following features required for 3U VME systems:

- A24/A16 addressing modes capability
- D16/D8 data transfer capability
- Automatic First-Slot-Detection
- Single level BR3 arbitration release-when-done option
- FAIR VMEbus arbitration option
- ACFAIL NMI option
- SYSFAIL IRQ option
- System controller functions (SYSCLK, Bus monitor, Power monitor)
- Compatibility with PEP 3U VME system addressing schemes
- Compatibility with PEP VME backplane design and feature set
- Compatibility with PEP backplane transceiver logic

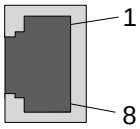
A table showing the pinout of the VME bus connector appears on the following page.

VME Bus Connector Pinout

Table 2-1: Pin Assignment J1/P1 VME

Pin Number	Pinrow A	Pinrow B	Pinrow C
1	D00	BBSY	D08
2	D01	BCLR	D09
3	D02	ACFAIL	D10
4	D03	BG0IN	D11
5	D04	BG0OUT	D12
6	D05	BG1IN	D13
7	D06	BG1OUT	D14
8	D07	BG2IN	D15
9	GND	BG2OUT	GND
10	SYSCLK	BG3IN	SYSFAIL
11	GND	BG3OUT	BERR
12	DS1	BR0	SYSRESET
13	DS0	BR1	LWORD
14	WRITE	BR2	AM5
15	GND	BR3	A23
16	DTACK	AM0	A22
17	GND	AM1	A21
18	AS	AM2	A20
19	GND	AM3	A19
20	IACK	GND	A18
21	IACKIN	SERA	A17
22	IACKOUT	SERB	A16
23	AM4	GND	A15
24	A07	IRQ7	A14
25	A06	IRQ6	A13
26	A05	IRQ5	A12
27	A04	IRQ4	A11
28	A03	IRQ3	A10
29	A02	IRQ2	A09
30	A01	IRQ1	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

2.4.3.2 Ethernet Connector and Pinout



The Ethernet interface is based on a PCI device from Intel; the Ethernet Controller 82559ERS.

The main features of the Ethernet are as follows:

- integrated IEEE 802.3 10Base T and 100Base TX compatible PHY
- glueless 32-bit PCI master interface
- compatible with driver software of the 82558 and 82557
- full duplex support at both 10 and 100 Mbps
- IEEE 802.3u Auto-Negotiation support
- 4 kB transmit and 3 kB receive FIFO's

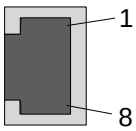
Ethernet Connector Pinout

The connector used for the 100BaseTX Ethernet interface is an RJ45 connector. The signals on this connector are as follows

Table 2-2: Ethernet RJ45 Pin Assignment

Pin Number	Signal
1	TX+
2	TX-
3	RX+
4	nc
5	nc
6	RX-
7	nc
8	nc

2.4.3.3 Serial Interfaces and Pinouts



Two serial ports (RS232) are provided by means of two 8-pin RJ45 connectors.

The RS232 serial interfaces named TERM and SER are 16C550 compliant and have 128-byte transmit and receive buffers. In addition to their other uses, the TERM port is used to interface with the bootstrap loader and the SER port is used to download software.

Electrically, the two serial ports are identical and they provide a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 115.2 KBaud.

The upper serial interface (SER) can also be configured to act as an RS485 interface. The configuration of the interface is achieved by setting the RS_CTL bit in the Control Register. Please refer to Table 4-14 in chapter 4.

Additionally, a module is available from *PEP* which provides an optoisolated half/full duplex RS485 interface. For this reason the onboard SER connector on the VMP1 baseboard is not equipped. Please contact *PEP* Support department for more information.

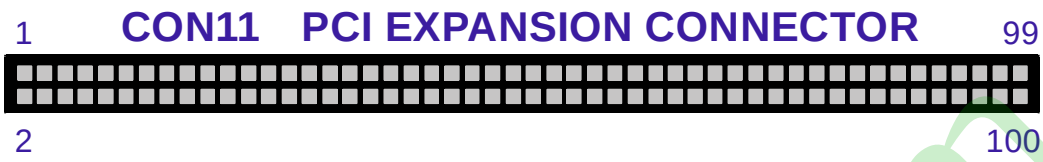
Pinouts of Serial Ports (RJ45 Connectors)

Table 2-3: Serial Port Pin Assignment

Pin Number	Signal	RS485	
		Signal Half-duplex	Signal Full-duplex
1	DSR	NC	-RxD
2	RTS	NC	NC
3	GND	GND	GND
4	TXD	+TRXD	-TxD
5	RXD	NC	NC
6	DCD	NC	+RxD
7	CTS	-TRXD	+TxD
8	DTR	NC	NC

2.4.3.4 PCI Expansion Connector and Pinout

Figure 2-5: PCI Expansion Connector



The PCI Expansion Connector provides the possibility to mount several transition boards above the VMP1 for adding special functionality which is not provided on the VMP1 main board or on the VME bus. All the PCI signals of the onboard PCI bus will be routed to this connector, so that a complete PCI bus is provided on this connector. In addition, almost the same number of ground and power pins (3.3V and 5V) as are on a CPCI P1 or PMC connector are provided. Examples of transition boards are:

- PMC carrier
- PC-MIP carrier
- IO board with Graphic interface, second Ethernet interface, SCSI etc.

A table showing the pinout of the PCI Expansion Connector appears on the following page.

PCI Expansion Connector (CON11) Pinout

Table 2-4: PCI Expansion Connector Pinout

Signal	Pin Number	Pin Number	Signal
GND 1)	1	2	SCL (I2C)
RST#	3	4	+3.3V 2)
+3.3V 2)	5	6	CLK2
CLK3	7	8	GND 1)
GND 1)	9	10	CLK4
INTB#	11	12	INTA#
INTD#	13	14	INTC#
+5V 3)	15	16	GNT#2
GNT#3	17	18	+5V 3)
+3.3V 2)	19	20	GNT#4
GND 1)	21	22	REQ#2
REQ#3	23	24	GND 1)
+5V 3)	25	26	REQ#4
AD31	27	28	AD30
AD29	29	30	+5V 3)
GND 1)	31	32	AD28
AD27	33	34	AD26
AD25	35	36	GND 1)
+3.3V 2)	37	38	AD24
C/BE3#	39	40	SDA (I2C)
AD23	41	42	+3.3V 2)
GND 1)	43	44	AD22
AD21	45	46	AD20
AD19	47	48	GND 1)
+5V 3)	49	50	AD18
AD17	51	52	AD16
C/BE2#	53	54	+5V 3)
GND 1)	55	56	FRAME#
IRDY#	57	58	GND 1)
+3.3V 2)	59	60	TRDY#
DEVSEL#	61	62	GND 1)
GND 1)	63	64	STOP#
LOCK#	65	66	+3.3V 2)

Table continued on following page

Table 2-4: PCI Expansion Connector Pinout

Signal	Pin Number	Pin Number	Signal
PERR#	67	68	+5V 3)
SERR#	69	70	GND 1)
+5V 3)	71	72	PAR
C/BE1#	73	74	AD15
AD14	75	76	+3.3V 2)
GND 1)	77	78	AD13
AD12	79	80	AD11
AD10	81	82	GND 1)
GND 1)	83	84	AD9
AD8	85	86	C/BE0#
AD7	87	88	+5V 3)
+3.3V 2)	89	90	AD6
AD5	91	92	AD4
AD3	93	94	GND 1)
GND 1)	95	96	AD2
AD1	97	98	AD0
+12V 4)	99	100	-12V 5)

Key

1) Ground
2) +3.3V
3) +5V
4) +12V
5) -12V

2.4.3.5 Serial Interface Expansion Connector and Pinout

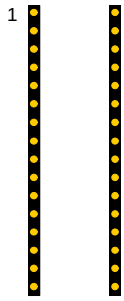
The serial interface expansion connector provides the capability to add different front end interfaces to the UART B signals. For example, an opto-isolated RS422/485 module (currently under development) may be plugged onto this connector.

Serial Interface Expansion Connector CON3 Pinout

Table 3-5: Serial Interface Expansion Connector (CON3) Pinout

Pin Number	Function	Function	Pin Number
1	GND	RTSB	2
3	RE	DE	4
5	RxD	TxD	6
7	CTS	DTR	8
9	SCL	SDA	10
11	+3.3V	VCC	12

2.4.3.6 Memory Expansion Connector



A 32-pin DIL600 socket is provided in order to make possible the addition of various memory expansion devices (with access time <120ns). The devices which have been tested and approved for this connector are as follows:-

DIL type Flash memory (up to 512 kB)

DIL SRAM (up to 512 kB) e.g. Samsung KM684000BLP-7

NVSRAM (up to 512 kB) e.g. DALLAS DS1250Y-100)

Eprom (up to 512 kB) e.g. 27C040

M-Systems DiskOnChip 2000 (up to 288 MB)

Note:

For the pinout of this connector please see Chapter 4, section 4.2.1

2.4.3.7 DEBUG Interface and Pinout

A JTAG/BDM interface is provided on the VMP1 for software debugging. The pinout of this connector is in accordance with the pinout of the most commonly used emulator probes.

Note:

As shipped, only the Altera onboard logic may be detected by means of the JTAG interface. If the JTAG interface requires to be re-configured for software debugging, please contact Support at *PEP Modular Computers* for assistance.

Debug Connector Pinout

Table 2-6: Debug Interface Connector (CON10) Pinout

Signal	Pin Number	Pin Number	Signal
TDO	1	2	NC
TDI	3	4	TRST#
NC	5	6	3.3V
TCK	7	8	NC
TMS	9	10	NC
SRESET#	11	12	NC
HRESET#	13	14	KEY (no pin)
CHKSTP#	15	16	GND

2.4.4 Digital Temperature Sensor (LM75)

The VMP1 also provides an onboard digital temperature sensor with a thermal watch-dog functionality (National Semiconductor LM75). This has various uses including, for example, calibration of the onboard RTC over a wider temperature range.

2.5 Special Board Features

2.5.1 Watchdog Timer

A watchdog timer is provided, which forces an NMI or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 4 steps with a resolution of 500 ms. If the watchdog timer is enabled, it cannot be stopped or reprogrammed.

Table 2-7: Watchdog Time Values

Watchdog Time Values
500 ms
1 s
1.5s
2 s

2.5.2 RTC (STC M41T56)

The Real Time Clock provides the following features:

- counters for seconds, minutes, hours, day, date, month and year.
- clock calibration by software
- low supply current for buffering with Gold Caps
- alternatively a battery may be placed on the board to buffer the RTC for a longer time
- it is also possible to buffer the power supply for the RTC via the VME-5V-Standby power line
- automatic leap year compensation
- precision: 35 ppm
- for greater precision or for temperature compensation the RTC can be adjusted in in steps of +4.068 or –2.034 ppm
- for temperature compensation, the onboard temperature sensor (LM75) may be used

2.5.3 Reset/Abort

There are also 2 push button switches with the function ABORT and RESET. The RESET button reinitializes the board via hardware.

The ABORT button initiates the NMI. In addition it is latched into a bit in the System Logic, the purpose of this is to differentiate between the NMI initiated from the ABORT Button and the NMI initiated from the watchdog. The positions of the Abort and Reset buttons on the Front Panel may be viewed in Figure 2-2.

2.5.4 Front Panel LED's

Three LED's with the colors red, green and yellow are provided on the front panel (please see Figure 2-2 on page 2-4) to give a quick indication of several key operating conditions:

- The red LED (H) is general purpose.
- The yellow LED (W) indicates WATCHDOG ACTIVE
- The green LED (U) has been preset to light on initialisation of the board. Afterwards it is available for general purposes

The general purpose LED's are programmable via a register in the System Logic.

3 additional LED's, all green, are provided to indicate Ethernet working conditions:

- Ethernet Link Integrity
- Ethernet Activity
- Ethernet Speed

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Chapter 3

Installation

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3. Installation

The VMP1 has been designed for easy installation. However, the following important-standard precautions must be observed. Some other important information is also set out below.

3.1 Board Installation

Slot Selection

The VMP1 is designed so that it may be used in any free slot of a 3U VME Backplane. It has an automatic first slot detection mechanism which configures it as a System Controller when placed in the far left slot.

When configured as the System Controller, it enables its system clock and arbiter in order to control the entire VME bus.

Default setting of the serial Interfaces: 9600 Baud, 8N1

On initial startup a message of greeting comes up.

When the VMP1 is invoked for the first time, a Bootstrap loader startup message comes up on the “term” serial port, which will provide you with some configuration information on the system and a command prompt for entering bootstrap loader commands. For a detailed description of these commands please see chapter 5 Bootstrap loader.

Caution!

Please switch off the VME system before installing the board in a free slot. Failure to do so could endanger your life/health and may damage your board or system.

Note:

Certain VME boards require bus master capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure your system is provided with an appropriate free slot to insert the board.

ESD Equipment!

Your VMP1 board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

PEP Advantage

The VMP1 is designed to be bootstrapped from the Flash device alone.

3.1.1 Front Panel I/O Connectors

Attention!

Due care should be exercised when connecting cabling in order to avoid damage to your connected device and/or the VMP1 board.

For pinouts of the Front Panel connectors, please see Chapter 2: Functional Description, sections 2.4.3.2 and 2.4.3.3

Chapter 4

Configuration

Configuration

4. Configuration

4.1 Jumper Settings

Please see Figures 2-3 and 2-4 in Chapter 2 to view the positions of the jumpers and resistors on the board.

4.1.1 Bootstrap Loader / Socket Jumper J1

The Jumper J1 is used to select the memory position from which the VMP1 fetches its boot code. It determines the address position of the onboard Flash window and the Flash/SRAM expansion socket (DIL600, 32-pin).

Table 4-1: Bootstrap Loader / Socket Jumper J1 Settings

J1	Meaning	Address Assignment	
Open	VMP1 fetches boot code from onboard Flash	Socket: Onboard Flash window:	0xFFF8 0000 - 0xFFFF FFFF 0xFFF0 0000 - 0xFFF7 FFFF
Closed	VMP1 fetches boot code from socket	Socket: Onboard Flash window:	0xFFF0 0000 - 0xFFF7 FFFF 0xFFF8 0000 - 0xFFFF FFFF

Note: The MPC8240 initially fetches its boot code from address 0xFFF0 0100!

4.1.2 RTC (Real-time clock) Calibration Output J2

Frequency test output is used for calibration of the onboard RTC. The RTC provides a 512 Hz frequency test signal for calibration purposes. Please refer to the datasheet of the ST M41T56 for detailed information (for position of J2 on the board please see figure 2-3).

Warning!

J2 must not be bridged.

4.1.3 Resistor Setting for Non-standard Socket Devices

The default pinout of this socket is designed for use with standard DIL Flashes and M-Systems DiskOnChip. As some devices have a different pinout, resistors must be set accordingly (please see figure 2-4 for an illustration of these resistors on the board)

Table 4-2: Resistor Setting for Various Non-standard Socket Devices

Used Socket Devices	R3	R6	R7	R8	R11	R12	R13
Flash (default)	Open	Open	Open	Set	Set	Open	Set
DiskOnChip (default)	Open	Open	Open	Set	Set	Open	Set
NVSRAM	Open	Open	Set	Open	Set	Set	Open
4 Mbit EPROM	Set	Set	Open	Open	Open	Open	Set

Note: All resistors are 0Ω

4.1.4 RS485 Termination (Onboard Interface Only)

When the VMP1 is using the onboard RS485 interface and is the last on the RS485 bus, then the RS485 interface must provide termination resistance. The purpose of J3 is to enable this line termination resistor (130 R).

Table 4-3: Jumper Settings for RS485 Termination

Termination	J3
ON	Set
OFF	Open

Additionally, the correct idle line potential must be provided at one location within the RS485 bus. J4 and J5 are used for this purpose. Pullup/Pulldown resistors are 380 Ohm each.

Note:

Ensure that the reference potential for the RS485 signals are set in one location only on the bus.

4.2 Pinouts

4.2.1 Flash Socket Type Selection

4.2.1.1 Socket Device Selection (Memory Expansion Socket IC8)

A range of different memory devices may be used on the DIL32 socket (e.g. Flashes, NVSRAM, M-Systems Disk-On-Chip, EPROM etc.).

Table 4-4: DIL 32 Pinout for Various Devices

Pin	4Mbit Flash	Disk OnChip	NV SRAM	4Mbit Eprom		4Mbit Eprom	NV SRAM	Disk OnChip	4Mbit Flash	Pin
1	A18	NC	A18	VPP		VCC	VCC	VCC	VCC	32
2	A16	NC	A16	A16		A18	A15	WE_	WE	31
3	A15	NC	A14	A15		A17	A17	NC	A17	30
4	A12	A12	A12	A12		A14	WE	NC	A14	29
5	A7	A7	A7	A7		A13	A13	NC	A13	28
6	A6	A6	A6	A6		A8	A8	A8	A8	27
7	A5	A5	A5	A5		A9	A9	A9	A9	26
8	A4	A4	A4	A4		A11	A11	A11	A11	25
9	A3	A3	A3	A3		OE_	OE_	OE_	OE_	24
10	A2	A2	A2	A2		A10	A10	A10	A10	23
11	A1	A1	A1	A1		CE_	CE_	CE_	CE_	22
12	A0	A0	A0	A0		D7	D7	D7	D7	21
13	D0	D0	D0	D0		D6	D6	D6	D6	20
14	D1	D1	D1	D1		D5	D5	D5	D5	19
15	D2	D2	D2	D2		D4	D4	D4	D4	18
16	GND	GND	GND	GND		D3	D3	D3	D3	17

4.2.2 Serial Interface Expansion Connector (CON3)

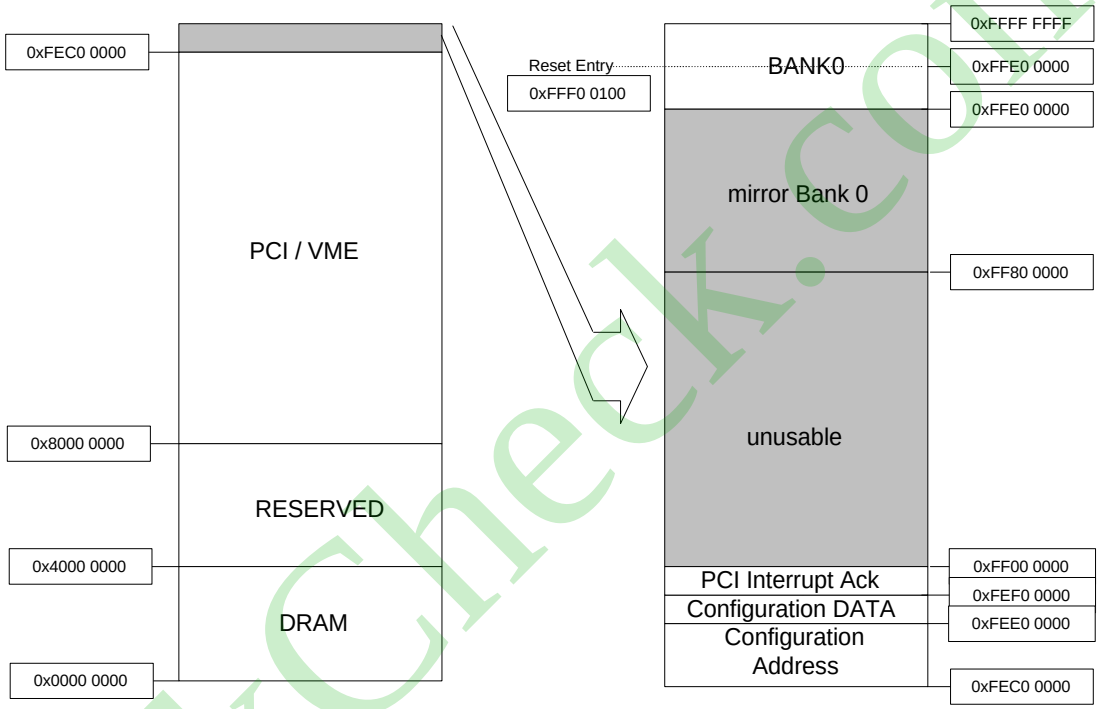
Table 4-5: RS Expansion Connector Pinout

Pin Number	Function	Function	Pin Number
1	GND	RTSB	2
3	RE	DE	4
5	RxD	TxD	6
7	CTS	DTR	8
9	SCL	SDA	10
11	+3.3V	VCC	12

4.3 Board Address Map

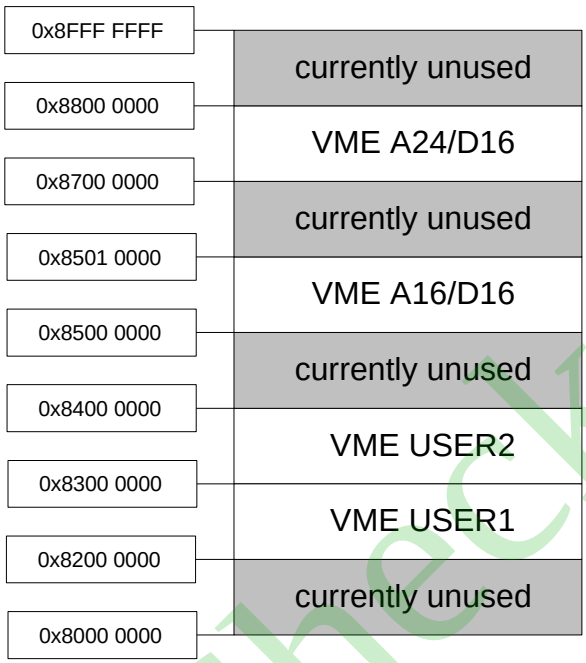
4.3.1 Address Map Overview

Figure 4-1: VMP1 Address Map, 2 MB 8-bit Bank



4.3.2 VME Address Area

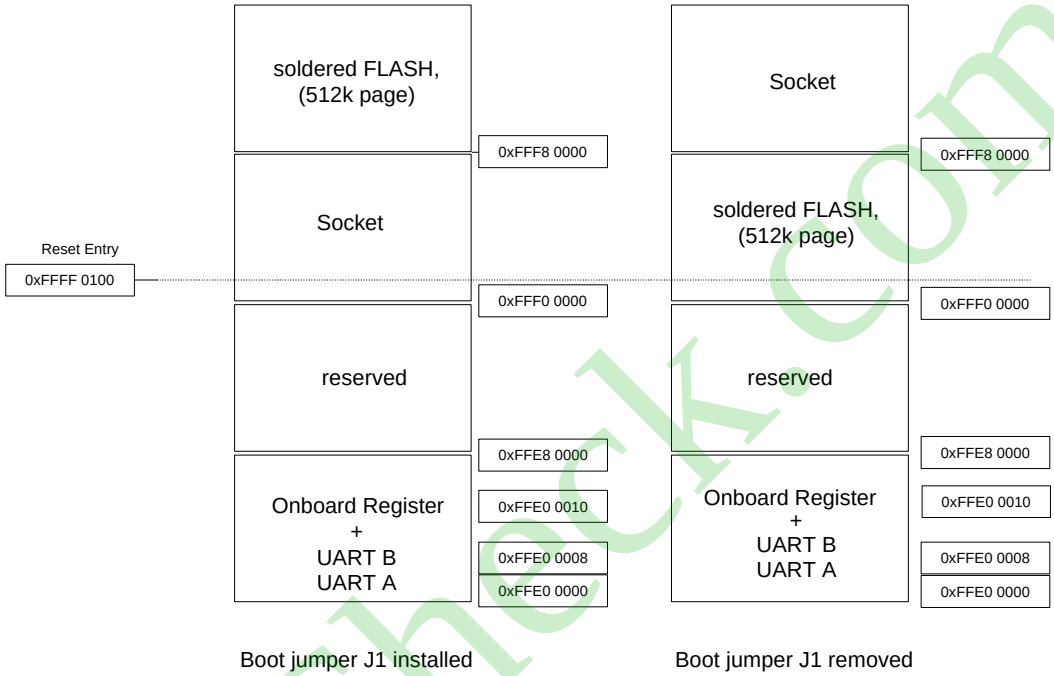
Figure 4-2: VME Address Area



VME bus slave address and VME IRQ mask are programmable inside the TUNDRA UNIVERSE II. Please refer to the VME slave manual chapter in the TUNDRA UNIVERSE II manual and the BSP documentation.

4.3.3 Onboard Device Addresses

Figure 4-3: VMP1 Device Address Map



Note:

- For write access to this address area (0xFFE0 0000-0xFFFF FFFF), it is only possible to use byte-wide write commands.
- When the memory expansion socket is used for NVSRAM, byte 0xFFF0 0000 (J1 installed) or byte 0xFFF8 0000 (J1 removed) is reserved for the output of post codes to the VMP1-Post. Data should not be stored at either of these locations.

4.3.4 Special Registers Overview

The Special Registers may be attached through read and write operation to the address space FFe8 0000-FFF0 0000

4.3.4.1 Board Control Registers

Table 4-6: Board Control Registers

Register	Address	Read/Write
Board-ID	FFe0 0010	R
Software Compatibility ID	FFe0 0012	R
Memory Configuration	FFe0 0014	R
Flash Bank Select	FFe0 0016	R/W
Watchdog Control Register	FFe0 0018	R/W
Control Register	FFe0 001a	R/W
Event Register	FFe0 001c	R/W
Board/Logic Revision	FFe0 001e	R

4.3.4.2 Board ID Register

Table 4-7: Board ID Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Board ID	FFe0 0010	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0

The Board ID can be used to identify the VMP1 in a VME system. The value for the VMP1 is 00h.

- **This register is READ ONLY**

4.3.4.3 Software Compatibility ID

Table 4-8: Software Compatibility ID

Register	Address	MSB	6	5	4	3	2	1	LSB
Software Compatibility ID	FFe0 0012	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

The Software Compatibility ID will signal to the software when differences in hardware require different handling by the software. This register is READ ONLY. It starts with the value 0x00 and will be incremented with each change in hardware (software sensitive only).

4.3.4.4 Memory Configuration Register

Table 4-9: Memory Configuration Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Memory Configuration	FFe0 0014	BJ	Res.	Res.	ECC	Res.	Res.	SZ1	SZ0

- Bits SZ0 and SZ1 are used to identify the soldered SDRAM size.
- Bit 2 and Bit 3 are reserved
- Bit 4 (ECC) is used to indicate that ECC is supported (1 = ECC enabled)
- Bit MSB (BJ) indicates the status of the BOOT JUMPER (jumper J1 for exchanging Socket and Flash Chip Select). 0 = boot jumper set, 1 = boot jumper removed

4.3.4.5 SDRAM Size

Table 4-10: SDRAM Size

SZ1	SZ0	Meaning
0	0	32 MB/1 Bank
0	1	64 MB/2 Banks
1	0	Reserved
1	1	Reserved

4.3.4.6 Flash Bank Select Register

Table 4-11: Flash Bank Select Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Flash bank select	FFe0 0016	Res.	Res.	Res.	Res.	FB3	FB2	FB1	FB0

The Flash bank select register is used to select the appropriate Flash bank. As 8-bit wide Flash memory may only be accessed through a 512 kB window; this is the only way to address a larger size Flash memory. Using bits FB0..FB3, 16 Flash banks can be selected (16x512 kB = 8 MB). The default value on startup of the VMP1 is 0x00.

4.3.4.7 Watchdog Control Register

Table 4-12: Watchdog Control Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Watchdog control	FFe0 0018	WD_EN	WD_R	Res.	WD_TRG	Res.	Res.	WDT1	WDT0

4.3.4.8 Watchdog Timeout Time

Bits WDT0 and WDT1 are programmed to select the Watchdog timeout value.

Table 4-13: Watchdog Timeout Time

WDT1	WDT0	Time
0	0	0,5s
0	1	1s
1	0	1,5s
1	1	2s

- Bits 2 and 3 are reserved
- Bit WD_TRG retriggers the watchdog timer. A “1” written to this bit sets the watchdog back to its start condition.
- Bit 5 is reserved
- Bit WD_R (Watchdog Route). If set to 0 (default), then the watchdog timer causes a reset, If set to 1, the watchdog timer will generate the NMI
- Bit 7: WD_EN: A “1” written to this bit starts the Watchdog. Once it has been enabled it cannot later be disabled.

4.3.4.9 Control Register

Table 4-14: Control Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Control	FFe0 001a	RS_CTL	Res.	Res.	S_RST	Res.	Res.	LED2*	LED1*

- Bits 0 – 1: A “1” written to these bits lights the LED’s (LED1* is the green LED of the top set on the front panel and LED2* is the red one)
- Bits 2 – 3 are reserved
- Bit S_RST: A “1” written to this bit initiates a Software Reset
- Bits 5 – 6 are reserved
- Bit 7: A “0” written to this bit configures the onboard SER connector to act as an RS232 interface. A “1” written to this bit configures the onboard SER connector to act as an RS485 interface (not optoisolated/half duplex)(default = 0)

Warning:

When setting bit 7 the user must ensure that the corresponding interface is also an RS485. A mismatch will risk damage to the VMP1 and/or the application.

4.3.4.10 Event Register

Table 4-15: Event Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Event	FFe0 001c	NLRST	Res.	Res.	Res.	Res.	PB2	Res.	WD

- Bit WD is used to indicate that a watchdog overrun has occurred (logic 1 if condition has occurred)
- Bit 1 is reserved
- Bit PB2 is used to indicate that the abort button has been pressed (logic 1 if this condition has occurred)
- Bits 3 - 6 are reserved
- Bit 7: ”NOT LRST” – this bit shows the status of the LRST pin of the TUNDRA UNIVERSE II (important for bootstrap loader).

4.3.4.11 Board / Logic Revision Register

Table 4-16: Board / Logic Revision Register

Register	Address	MSB	6	5	4	3	2	1	LSB
Board revision	FFE0 001e	LR3	LR2	LR1	LR0	BR3	BR2	BR1	BR0

The Board Revision Register may be used to identify the hardware and logic status of the board by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each redesign / logic release.

- **This register is READ ONLY.**

4.3.4.12 UART A / Registers

For a detailed description please refer to the EXAR XR16C 2850 DUART manual.

The UART A occupies the following addresses:

Table 4-17: General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR)

Read Mode	Write Mode	Address
Receive Holding Register	Transmit Holding Register Interrupt Enable Register	FFe0 0000 FFe0 0001
Interrupt Status Register	FIFO Control Register Line Control Register (LCR) Modem Control Register	FFe0 0002 FFe0 0003 FFe0 0004
Line Status Register	--	FFe0 0005
Modem Status Register	--	FFe0 0006
Scratchpad Register	Scratchpad Register	FFe0 0007

Table 4-18: Baud Rate Register Set (DLL/DLM)

Read Mode	Write Mode	Address
LSB of divisor latch	LSB of divisor latch	FFe0 0000
MSB of divisor latch	MSB of divisor latch	FFe0 0001

Table 4-19: Enhanced Register Set

Read Mode	Write Mode	Address
Trigger Level Register	Trigger Level Register	FFe0 0000
Feature Control Register	Feature Control Register	FFe0 0001
Enhanced Feature Register	Enhanced Feature Register	FFe0 0002
Enhanced Mode Select Register	Enhanced Mode Select Register	FFe0 0007
Xon-1	Xon-1	FFe0 0004
Xon-2	Xon-2	FFe0 0005
Xoff-1	Xoff-1	FFe0 0006
Xoff-2	Xoff-2	FFe0 0007

4.3.4.13 UART B / Registers

For a detailed description please refer to the EXAR XR16C 2850 DUART manual

The UART B occupies the following addresses:.

Table 4-20: General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR)

Read Mode	Write Mode	Address
Receive Holding register	Transmit Holding Register	FFe0 0008
--	Interrupt Enable Register	FFe0 0009
Interrupt Status register	FIFO Control Register	FFe0 000a
--	Line Control Register	FFe0 000b
--	Modem Control Register	FFe0 000c
Line Status register	--	FFe0 000d
Modem Status register	--	FFe0 000e
Scratchpad register	Scratchpad Register	FFe0 000f

Table 4-21: Baud Rate Register Set (DLL/DLM)

Read Mode	Write Mode	Address
LSB of divisor latch	LSB of divisor latch	FFe0 0008
MSB of divisor latch	MSB of divisor latch	FFe0 0009

Table 4-22: Enhanced Register Set

Read Mode	Write Mode	Address
Trigger level register	Trigger level register	FFe0 0008
Feature Control register	Feature control register	FFe0 0009
Enhanced feature register	Enhanced feature register	FFe0 000a
Enhanced mode select register	Enhanced mode select register	FFe0 000f
Xon-1	Xon-1	FFe0 000c
Xon-2	Xon-2	FFe0 000d
Xoff-1	Xoff-1	FFe0 000e
Xoff-2	Xoff-2	FFe0 000f

4.3.5 IRQ Routing

Table 4-23: Serial IRQ's

IRQ Name	Source
S_IRQ0	Reserved
S_IRQ1	UART-A
S_IRQ2	UART-B
S_IRQ3	INTA# (PCI)
S_IRQ4	INTB# (PCI)
S_IRQ5	INTC# (PCI)
S_IRQ6	INTD# (PCI)
S_IRQ7	Temperature sensor interrupt
S_IRQ8	LINT0# / VME Interrupt level 1 and 2
S_IRQ9	LINT1# / unused
S_IRQ10	LINT2# / VME Interrupt level 3 and 4
S_IRQ11	LINT3# / VME Interrupt level 5 and 6
S_IRQ12	LINT4# / VME Interrupt level 7 + SYSFAIL
S_IRQ13	LINT5# / VME ACFAIL
S_IRQ14	LINT6# / 4 location monitors
S_IRQ15	LINT7# / 4 mailboxes

4.3.6 Real-time Clock

Access to the RTC is effected via the I2C bus. The RTC uses address 0xD0

For more detailed information please refer to the manuals for the ST - Microelectronics M41T56 and the Motorola MPC 8240 (I2C - Bus).

Table 4-24: Register Map RTC M41T56

Address	D7	D6	D5	D4	D3	D2	D1	D0	Function/Range in BCD Format
0	ST	10 Seconds			Seconds				Seconds / 00-59
1	X	10 Minutes			Minutes				Minutes / 00-59
2	CEB	CB	10 Hours		Hours				Century 0-1/Hour 00-23
3	X	X	X	X	X	Day			Day / 00-07
4	X	X	10 Date		Date				Date / 01-31
5	X	X	X	10 M.	Month				Month / 01-12
6	10 Years				Years				Year / 00-99
7	OUT	FT	S	Calibraton					Control

Meanings of abbreviations in Table 4-24

CEB = Century enable bit

CB = Century bit

FT = Frequency test bit

OUT = Output level

ST = Stop bit

S = Sign bit

Note:

When the RTC has once been stopped due to low voltage, it is necessary to re-initialize the “Seconds” “Minutes” and “Hours” registers before it will run again.

4.3.7 EEPROM

Access to the EEPROM is effected via the I2C bus of the MPC8240. The EEPROM uses the I2C address 0xA0.

For more detailed information please refer to the manuals for the MICROCHIP 24LC16B and the MOTOROLA MPC8240 (I2C bus).

4.3.8 Digital Temperature Sensor

Access to the onboard temperature sensor is effected via the I2C bus of the MPC8240. The EEPROM uses the I2C address 0x90.

For more detailed information please refer to the manuals for the National Semiconductor LM75 and the MOTOROLA MPC8240 (I2C bus).

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Chapter 5

Bootstrap Loader

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5. Bootstrap Loader

The VMP1 Bootstrap Loader is a standalone software located in the Flash memory which allows the user to safely update the contents of the Flash and delay the boot process for a specified time.

The Bootstrap Loader has the capability to program Flash memory from “MOTOROLA S-RECORDS” or from an absolute memory address. If the programmed image does not work, the Bootstrap Loader can be re-entered. The memory contents can be examined and another programming cycle initiated.

The Bootstrap Loader is delivered already installed in soldered Flash.

Please read this user manual before reprogramming any Flash memory.

Warning!

When programming Flash memory, please do not press the RESET button or switch off the mains power under any circumstances! Doing so may damage the Bootstrap Loader and would consequently leave the board unusable due to corrupt Flash contents.

However, the ABORT button may be used to cancel a running operation safely.

5.1 System Operation

5.1.1 Startup

After system reset, the Bootstrap Loader is started. It searches the Flash memory area for a valid start key. If this start key is found, the Bootstrap Loader checks the 'BootWaitTime' from serial EEPROM. If the entry is valid, the continuation of the boot process is delayed for a period during which the green front panel LED flashes to indicate that the system is alive but waiting for continuation. If the entry is not valid, a default of 5 seconds is used. After the BootWaitTime has passed, the program in Flash is downloaded and started.

The Bootstrap Loader has two modes of operation: non-interactive start mode as described above and the interactive command mode.

For normal board operation, only the non-interactive start mode is used to start a program in Flash. This happens automatically without any user interaction. The interactive command mode is used to re-program the Flash memory contents or change the BootWaitTime.

The serial term port operates at 9600 Baud, 8 bits / character, 1 stop bit and no parity by default.

5.1.2 Entering the Command Mode

There are two possible reasons for entering the Bootstrap Loader command mode:

- If no valid start key is found, the Bootstrap Loader command mode is entered automatically.
- If the user wants to enter the Bootstrap Loader manually, e.g. for re-programming the Flash contents, the ABORT button on the front panel must be used.

Important!

The ABORT button must not be pushed until the green LED is lit, because this button generates an NMI, and the exception vector tables must be initialized correctly to serve this NMI.

However, the ABORT button must be pushed before the green LED stops flashing (BootWaitTime), since the system control is transferred to the downloaded binary image afterwards. The LED is cycled every 0.25 sec. so if 1 second is specified as BootWaitTime, the LED will only flash twice.

CTRL-x deletes the complete input line while CTRL-a restores the last input line on the command I/F.

5.1.3 Programming a New Binary Image to Flash Memory

Preparing the Image

The image must be compiled / linked to run from the Flash base address 0x0 of the CPU. The image must contain executable PPC code at offset 0x100, as is usual for ROM/Flash images.

A binary image must be converted to Motorola S-records or loaded to a VME memory board with battery backup, Flash or EPROM population.

Programming with Motorola S-Records

Programming is done with the *If* command.

The *If* command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

The checksum of every record except end records is checked. Bad records are rejected by the Bootstrap Loader. The address range of every record is also checked; records that try to overwrite the Bootstrap Loader are rejected. Additionally, every record must match the programmable area exactly. To give the user an overview of the available ranges, the startup banner includes address information.

In the case of the VMP1 the Flash addresses are only “virtual”. The downloaded image is copied to RAM during startup and is executed there. For this reason images which require to be programmed in should start at the address 0×0.

Note:

The image must start at the absolute address 0×0 and must contain executable PPC code at the absolute address 0×100

If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses. If no switch to another record type is included it must be ensured that the code is not larger than the address range covered.

Important!

The ’If’ command cannot be used to program Motorola S-records to RAM areas.

For sending programming data, the lower *(term)* or upper *(ser0)* RJ45 front panel connectors can be used. The *ser0* port is preferable, because in this configuration it is possible to monitor the progress of the operation via the *term* port. In any case, the user LED flashes slowly while downloading to give feedback of the usual kind.

If not specified otherwise, sectors which are not touched by the programming operation are not erased. If you want to erase all sectors while programming, the '-c' option can be specified along with the *If* command. This is useful for software which searches memory during startup and should not find any old modules, for example OS-9.

Make sure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, make sure that your host does not stop transmission after a number of lines (e.g. OS-9: use the 'nopause' attribute).

Serial parameters can be modified with the *pf* command.

Monitoring the Programming Progress

In both examples, the programming can be monitored via the *term* port. The characters which are displayed have the following meaning:

- r Read S-record; valid and in range
- t Protected sector touched
- e Erase sector
- c Copy to buffer, program later
- p Program record

None of the above characters indicate an error. The first sector (which includes the first instruction to be executed) and the last sector (which includes the Bootstrap Loader itself) are protected. These sectors are not immediately programmed like the other sectors. The contents of these protected sectors are buffered in RAM and programmed at the end of the operation. This is done to limit the amount of time the Bootstrap Loader itself is not in Flash or not startable, because if the Bootstrap Loader crashes during this critical period of time, it will not start again afterwards.

Warning!

When programming Flash memory, please do not press the RESET button or switch off the mains power in any circumstances! Doing so may damage the Bootstrap Loader and would consequently leave the board unusable due to corrupt Flash contents.

However, the ABORT button may be used to cancel a running operation safely.

The parameter '-q' suppresses all messages and warnings except error messages.

Programming via the *term* port is also supported, but in this case programming of the loader is quiet by default. The progress of this process cannot be monitored directly, since only the green front panel LED (U) flashes while programming is in progress.

It is recommended that programming is undertaken via the *ser0* port.

Important!

Feedback is provided to the operator, however, please note that programming may take several minutes.

If the process must be aborted, press the ABORT button and try again. However, on CPU's without an ABORT button the process cannot be aborted.

Programming from an Absolute Address

The second way to program Flash memory is to program it from an absolute address. The image to be programmed must be located in a visible address range, for example on the VMEbus. A memory card with battery-backup, Flash or EPROM can be used to hold the image to program. If we assume that the image is located at 0x87000000 and is 0x123456 bytes large we must type the following at the command prompt of the Bootstrap Loader:

```
lf -m=87000000 -l=123456
```

The characters which are now displayed have the same meaning as if we are programming from S-records, but the time needed for each step to be completed may be longer because the loader tries to program with the largest possible block size that it can manage.

Again, '-c' can be used to clear untouched sectors.

Warning!

Quiet operation is not supported, and also it is not possible to specify any offset.

Please note also that programming cannot be canceled with ABORT.

5.1.4 BootWaitTime

The command *bw* can be used to display/change the current BootWaitTime. Available delays are 1-2-5-10-20-50 seconds. CPU's without a user LED or without an ABORT button have a BootWaitTime of at least 5 seconds. In this case, the Bootstrap Loader will reject a BootWaitTime setting of 1-2 seconds.

The BootWaitTime value is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.

Important!

If the CRC of the Boot section is not valid, changing the BootWaitTime has no effect because the bw command does not validate an invalid CRC in order to avoid undesired side effects. In this case, a default timing of 5 seconds is always used.

To validate an invalid CRC, the appropriate utility from an operating system must be used or, alternatively, the line *bw -f* must be issued.

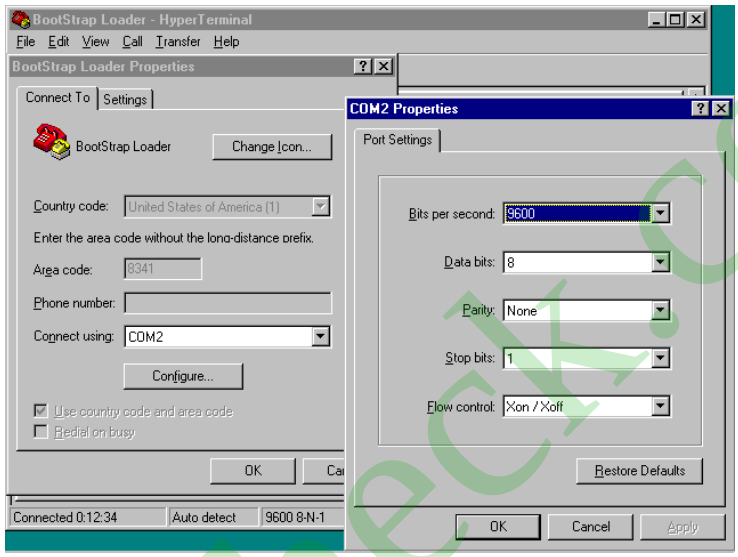
Warning!

Please note that validation with the 'bw -f' command may validate invalid entries, with adverse consequences.

5.1.5 Example Using Hyperterminal under Windows 95/Windows NT

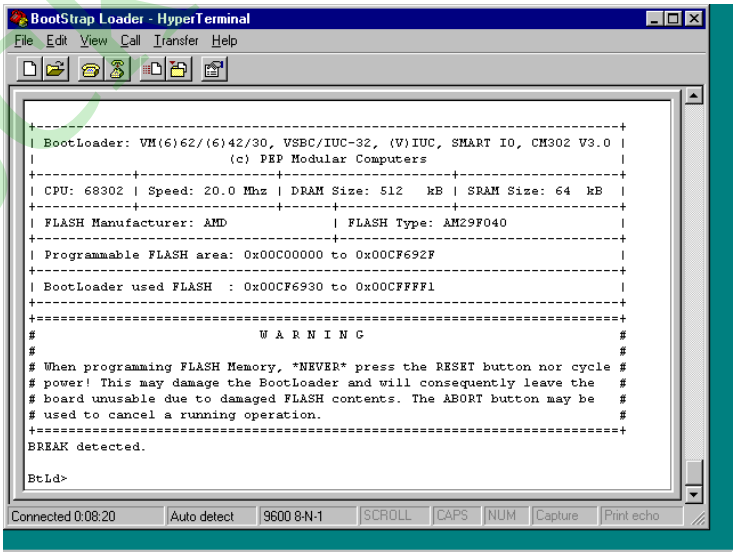
The host is assumed to be a PC with Windows 95 or Windows NT. A serial cable is used to connect the term port of the board to be programmed to COM2 of the PC. Additionally, we assume that we want to program a MOTOROLA S-record built for the Flash address of the board. The serial connection runs at the default configuration of 9600 Baud with no parity and one stop bit. The properties should appear as follows:

Figure 5-1: Setting of COM2 Properties



After entering the Command Mode the following screen should appear:

Figure 5-2: Screen after Entering the Command Mode



Enter 'lf' on the target. The target now waits until the MOTOROLA S-records have been transferred over the term. Select **Transfer/Send Text File** dialogue box and select the file containing the MOTOROLA S-records.

Figure 5-3: Select Transfer/Send Text File Dialogue Box

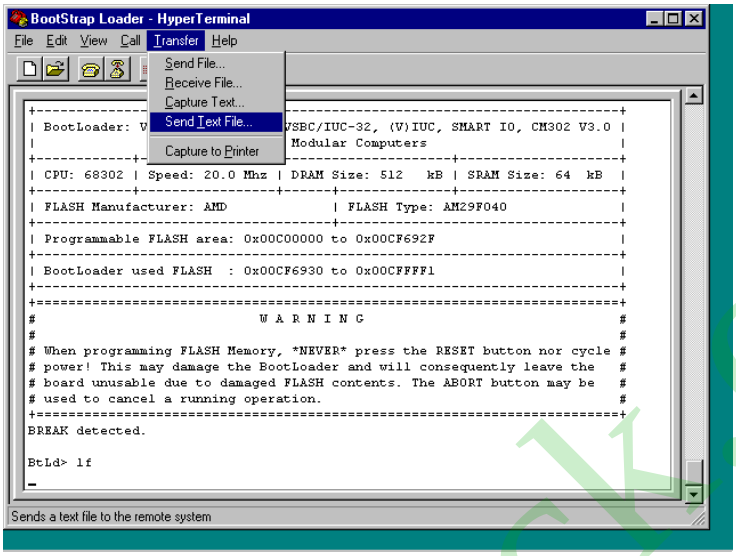
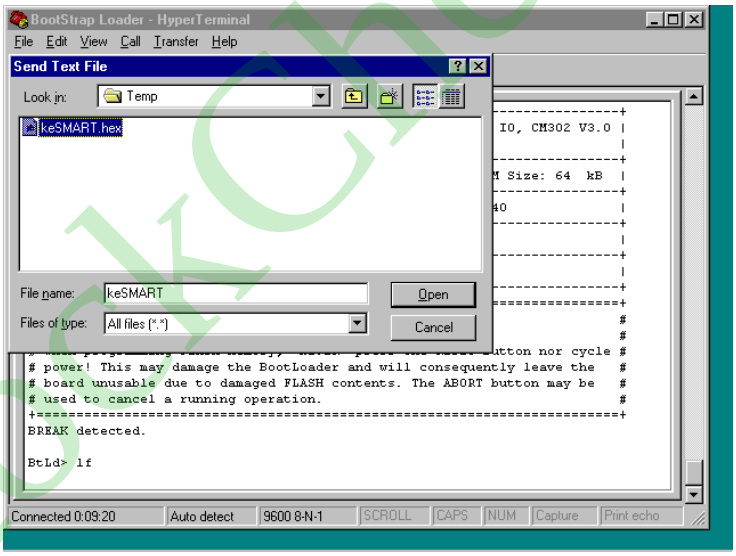


Figure 5-4: Selecting the MOTOROLA S-Records File



After selecting **Open** the dialogue box disappears and the MOTOROLA S-records are transferred. As soon as the complete file is sent, the prompt of the Bootstrap Loader appears again.

Important!

No status information is displayed.

5.2 Commands

5.2.1 Boot Wait

Syntax

```
bw [<time>| -f]
```

Description

Without parameters, *bw* displays the current setting.

The parameter <time> may be set to 1, 2, 5, 10, 20 or 50, which signifies the waiting time in seconds. No values other than these are supported, while the option '-f' has the following meaning:

- '-f' face CRC update.

Important!

CPU's without a user LED or without an ABORT button have a BootWaitTime of at least 5 seconds. The Bootstrap Loader will refuse to set a BootWaitTime of 1-2 seconds.

5.2.2 Load Flash

Syntax

```
If [-o[=]<offset>] [-u] [-q] [-c] [-m[=]<adr> -l[=]<len>]
```

Description

Without parameters, the Flash is loaded using S-records via the *term* port.

The parameter '<offset>' is a signed 32-bit offset which is added to every record and can be used to move the S-records to the Flash position.

Important!

This option must be selected if the S1 or S2 records are used.

- '-u' must be used to download over *ser0.*
- '-q' suppresses all messages except error messages.
- '-c' clears all untouched sectors and leaves no old code fragments.

For a Load Flash from an absolute address, the -m / -l options must be used.

Important!

On CPU's without a ser0 serial connection the Bootstrap Loader will refuse a command including the '-u' option.

5.2.3 Memory Display

Syntax

```
md [<adr>]
```

Description

Without parameters specified, the Flash contents starting at the beginning of the programmable Flash area are displayed. This function is not limited to Flash and other address ranges can be specified.

Important!

The first instruction to be executed in Flash is not identical to the one to be executed first from the programming source (S-records memory block).

5.2.4 Port Format

Syntax

```
pf [<port> [<baud>][/[<bitschar>][/[<parity>][/<stops>]]]]
```

Description

Without parameters specified, the current serial port settings are displayed.

- <port> specifies the serial port. Valid values are *term* or *ser0.*
- <baud> specifies the baud rate. The values 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400 and 115200 Baud can be specified.
- <bitschar> specifies the bits / character. Valid values are 7 or 8.
- <parity> specifies if parity should be checked / generated. The value n specifies none, o for odd and e for even parity.
- <stops> specifies the stopbits which will be generated. Valid values are 1 or 2.

Important!

No spaces are permitted between the options. Options must be separated with a slash. Not all options must be specified, but the '/' characters must be present to distinguish the different options from each other. The sequence can be aborted after every option.

On CPU's without a ser0 serial connection the Bootstrap Loader will refuse setting ser0 port parameters and will not display ser0 port parameters.

Examples

Setting *term* to 300 Baud, 7 Bits/char, odd parity and 2 stopbits:

```
pf term 300/7/o/n
```

Set the bits / character field to 7 for *ser0* only:

```
pf ser0 /7
```

Set the stopbits field to 2 for ser0:

```
pf ser0 ///2
```

5.2.5 Reset System

Syntax

`rs`

Description

This command exits the Bootstrap Loader and resets the system. It terminates the Bootstrap Loader command mode and resets the entire system, generating a system reset with the onboard watchdog.

5.2.6 Help

Syntax

`?` or *`help`*

Description

This command prints the online help page. The display of the help text varies between the different CPU's reflecting their differences.

5.2.7 PCI Bus Configuration

Syntax

Pci

Description

Displays the PCI configuration. This includes assigned addresses in memory, the I/O space and the assigned interrupt line.

5.3 Plug and Play

On the VMP1 the Bootstrap Loader includes "Plug and Play" functionality. This ensures that the board is completely initialized and that all resources necessary for PCI devices (addresses, interrupts etc.) are assigned automatically. This important feature has the advantage that conflicts do not arise when PCI devices are added or removed. Furthermore, the OS itself does not include the board initialisation code.

5.4 Porting an Operating System to the VMP1

The image for the absolute address 0×0 should be linked with an entry point at the absolute address at 0×100.

One should not attempt to reassign the PCI BAR registers. The assigned values should be read back and these should always be used in the drivers.

The “interrupt line” field in the PCI configuration header is initialized with the IRQ line number to which the INTA of the device is routed.

It is not necessary to rewrite the “EUMBBAR” field in the KAHLUA (MPC 8240) configuration space as this has already been done by the Bootstrap Loader. The existing value should be used.

Downloaded images are never executed from the Flash due to the fact that on the VMP1 it is paged . The programmed image is always downloaded to SDRAM, the absolute address 0×0 being downloaded first. There is no configuration option available to amend this process. If it is necessary to re-locate the image to another address after download, simply add a small assembly routine at the beginning of the code which will move the image to the correct address.

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Appendix A

VMP1-IO1 Module (Optional)

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VMP1-IO1 Module (Optional)

A Overview

The *PEP* VMP1-IO1 module has been designed to provide the VMP1 user with an effective gateway to the world of PMC modules. This additional capability opens up the broadest range of expansion possibilities.

PMC modules are renowned for their flexibility and versatility of use. They afford the user wide ranging system-independent solutions by means of easily interchanged or upgraded mezzanine add-on modules. The *PEP* VMP1-IO1 has been designed to maximize the advantages provided by PMC modules in a 3U environment.

A special feature of the VMP1 is the ability to cascade two of these IO1 modules on top of one another. This means that the VMP1 is able to carry any two PMC modules. Tremendous advantages in terms of expandability and flexibility are thus made available to the user as a result of the addition of this capability to the board's many outstanding features.

The VMP1-IO1 is a 3U non-intelligent, passive CPCI carrier board with one PMC slot.

Some of the Outstanding Features of the VMP1-IO1

- 32 Bit / 33MHz PCI Bus on the PMC side
- it supports the Interrupts INTA, INTB, INTC and INTD
- it supports all the signals of the PCI Bus on its connectors Jn1 (CON2), Jn2 (CON3)
- The connectors which connect the mezzanine board with the carrier include all the signals of a 33MHz, 32-bit, multi-master PCI bus, the power rails for 5V, 3.3V, V(I/O) and other specialised signals for Board Detection.

Features of the *PEP Modular Computers*' PMC modules

PEP Modular Computers' PMC modules are operable in both CompactPCI and VME systems. They offer all the key benefits of PC I/O technology, namely:

- low cost solutions
- high performance
- a processor independent local I/O bus
- a broad range of I/O peripheral devices

PEP Modular Computers' PMC modules may be installed on a variety of different carrier boards, including:

- CompactPCI 3U/6U: CPU CP302, CP600, CP602, CP610, CP611, CP612
- CompactPCI PMC carrier boards such as the CP390 and CP690
- VME 3U: VMP1 by means of the VMP1-IO1 module

B Board Interfaces

PCI Expansion Connector

The PCI expansion connectors CON2/CON3 provides all the necessary signals for data transfer as defined by PCI Specification Rev. 2.1.

PMC Interface

The PMC interface provides an easy way to extend the VMP1 via the wide array of interfaces and functions which are available on PMC modules produced by the entire range of PMC vendors. PMC connectors provide a 32-bit wide PCI data path with a speed of up to 33MHz which is routed to the onboard connectors Jn1 and Jn2. These connectors also provide the power supply for the PMC module. The interface has been designed to comply with the IEEE 1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor.

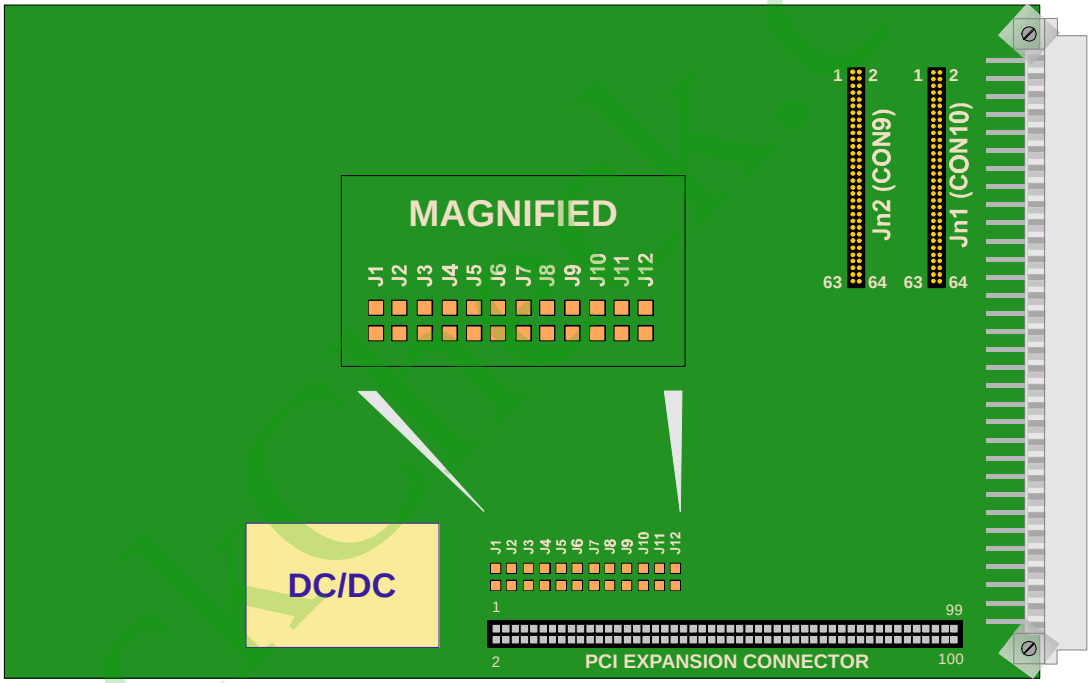
Power Supply

The onboard DC/DC converter of the VMP1-IO1 also produces 3.3V supply voltage from the 5V provided on the VME backplane. This is necessary in order to create compatibility with the PMC modules whose power consumption is in excess of what the baseboard (VMP1-IO1) can provide.

C Board Layout

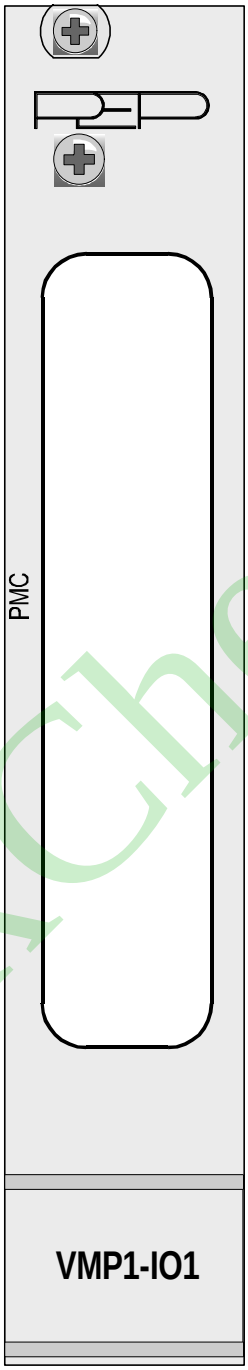
The VMP1-IO1 has two onboard connectors (CON9 and CON10) which provide all the PCI signals and the power supply for the PMC module.

Figure A-1: Board Layout (Front View)



D VMP1-IO1 Front Panel

Figure A-2: VMP1-IO1 Front Panel



The VMP1-IO1 front panel is provided with a window for the insertion of a PMC module bezel.

E Technical Specifications

Table A-1: VMP1-IO1 Specifications

VMP1-IO1	Specifications
PCI-Standard	Compliant with PCI 2.1
Signaling Voltage	PMC-Side: 5V signaling
Connectors	PMC Jn1 (CON4) and Jn2 (CON5) connectors
Mechanical Compliance	IEEE 1101.10 CMC IEEE P1386/Draft 2.0 (with minor exceptions)
Temperature Range	Operation: • -40° to +85°C Storage: • -55° to +85°C
Operating Humidity	5 – 95% (non condensing)
Vibrations and Broad-Band Random Vibration	IEC68-2-6 compliant IEC68-2-64
Shocks: Permanent Shocks Single Shock	 IEC68-2-29 IEC68-2-27
Board Dimensions	Single-height Eurocard: 100 mm x 160 mm 1 x 4 HP slot
Board Weight	114 grams

F Board Installation

In order to keep the installation process as simple and easy as possible please follow the recommended order of work:

1. Instal the PMC module on the VMP1-IO1
2. Instal the package, VMP1-IO1 plus PMC module, on the baseboard (in this case the VMP1)

ESD Equipment!

Your carrier board and PMC module contain electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

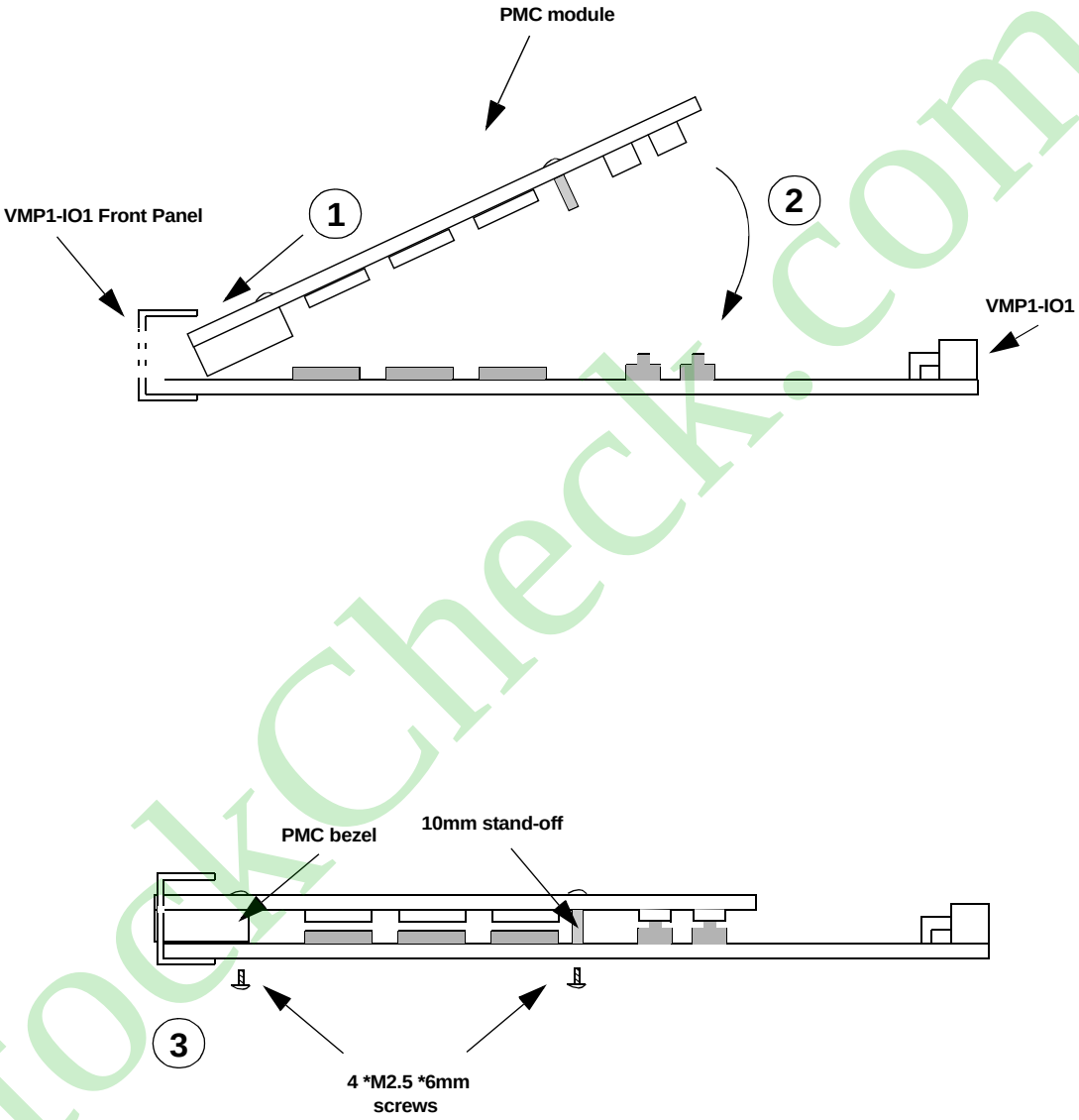
Installation of the VMP1-IO1 Module on the VMP1 Baseboard

3. Place the VMP1-IO1 exactly above the VMP1
4. Plug them togethor
5. Use 4 screws (2.5 × 6 mm) to secure the board to the VMP1

PMC Module Installation

6. Place the EMC gasket on the bezel of your PMC-Module
7. Push the PMC bezel into the window of the front-panel of the VMP1 and plug the connectors together.
8. Use three screws (M2.5 × 6mm) to secure the module to the board

Figure A-3: Installation Diagrams



G Pinouts

G1 Jn1 (CON4) Pin Assignment

Table A-2: Jn1, 32-bit PCI

Pin Number	Signal Name	Signal Name	Pin Number
1	TCK	-12V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD*	10
11	Ground	PCI-RSVD*	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

G2 Jn2 (CON5) Pin Assignment

Table A-3: Jn2, 32-bit PCI

Pin Number	Signal Name	Signal Name	Pin Number
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD*	8
9	PCI-RSVD*	PCI-RSVD*	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	3.3V	BUSMODE4#	16
17	PCI-RSVD*	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3.3V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	Ground	PMC-RSVD	64

H Jumper Setting

The jumper settings of the IO1 module depend on the module's position relative to the VMP1 and other modules, if any (please see Figure A4 below).

Table A4: IO1 Jumper Settings for Different Module Positions

	IDSEL			Clock			GNT#			REQ#		
	J12	J11	J10	J1	J2	J3	J4	J5	J6	J7	J8	J9
Position 1	Set	Open	Open	Set	Open	Open	Set	Open	Open	Set	Open	Open
Position 2	Open	Set	Open	Open	Set	Open	Open	Set	Open	Open	Set	Open
Position 3	Open	open	Set	Open	Open	Set	Open	Open	Set	Open	Open	Set

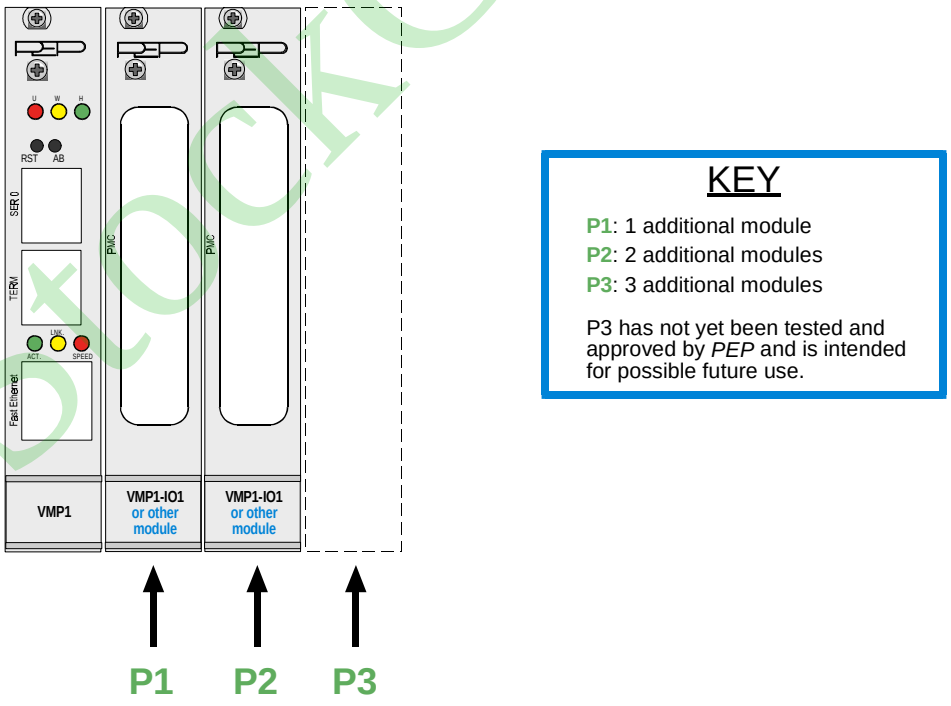
Note:

Position 1 refers to the settings applicable when 1 module (IO1 or other) is attatched to the VMP1.

Position 2 refers to the settings applicable when 2 modules (IO1 or other) are attatched to the VMP1.

Position 3 refers to the settings applicable when 3 modules (IO1 or other) are attatched to the VMP1.
Important!: Position 3 has not yet been tested and approved by *PEP* and is not recommended for use in this issue of the manual.

Figure A-4: Cascading of IO1 (or other) Modules onto the VMP1



Appendix B

VMP1-Post (Optional)

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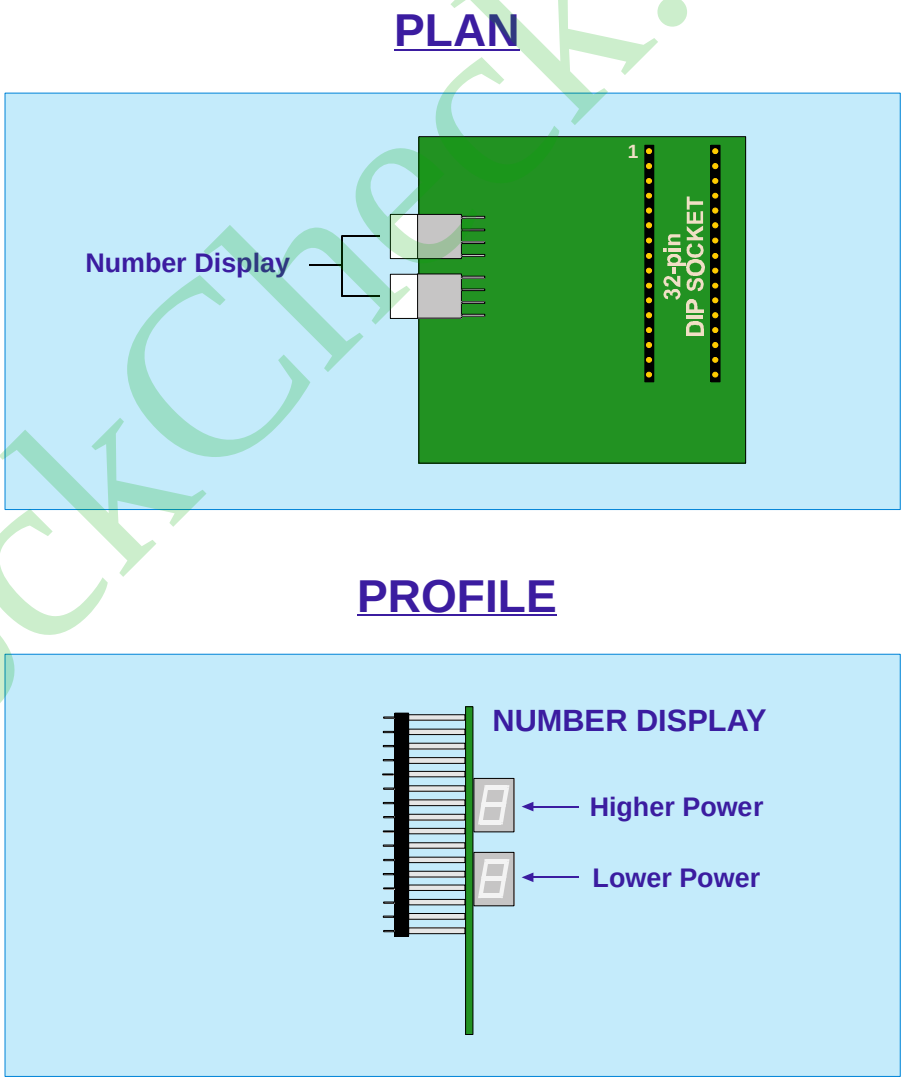
VMP1-Post (Optional)

Board description

The VMP1-Post is an optionally available tool which is used for hardware and software debugging. During the startup process of the VMP1 it provides the user with information about the status of the boot process by means of a message code similar to the post codes on the Intel PC. ***Please note that a Postcode reference list setting out the meanings of the number codes is available from the local sales office .*** When the board has completed the startup process, the VMP1-Post may be used to provide debug information for software development. The programmer can, therefore, define his own debug code and send it to the VMP1 by making a byte write command to the first address of the socket memory area. This address is 0xFFF0 0000 when the boot jumper J1 of the VMP1 is set and 0xFFF8 0000 when the boot jumper is open.

Figure B-1: Plan and Profile Views of VMP1 POST Module



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Appendix C

Optoisolation RS485 Module (Optional)

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Optoisolation RS485 Module (Optional)

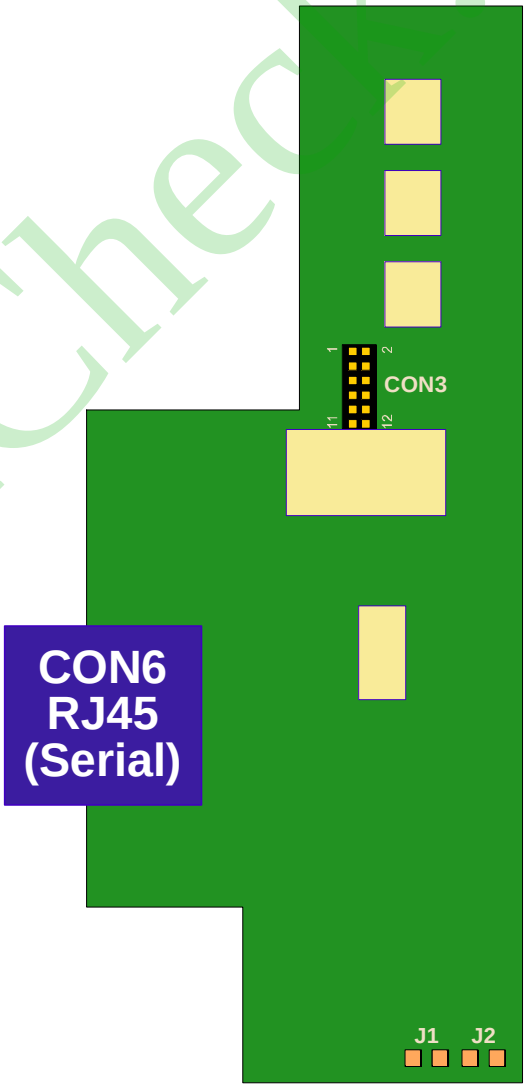
Board description

On the VMP1 it is possible to utilize a transition module which provides optoisolated RS485 functionality (half and full duplex).

Users who require an optoisolated version of the VMP1 are supplied with a customized VMP1 on which the standard RJ45 connector is omitted and also with this module which comes with a substitute RJ45 connector routed through optoisolation circuitry on the module.

The module has been designed so that it does not increase the board width, which remains unchanged at 4TE with the module in place.

Figure C-1: View of underside of RS485 Module



Please note that this diagram is not to scale with other board diagrams

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Appendix D

JTAG Subsystem

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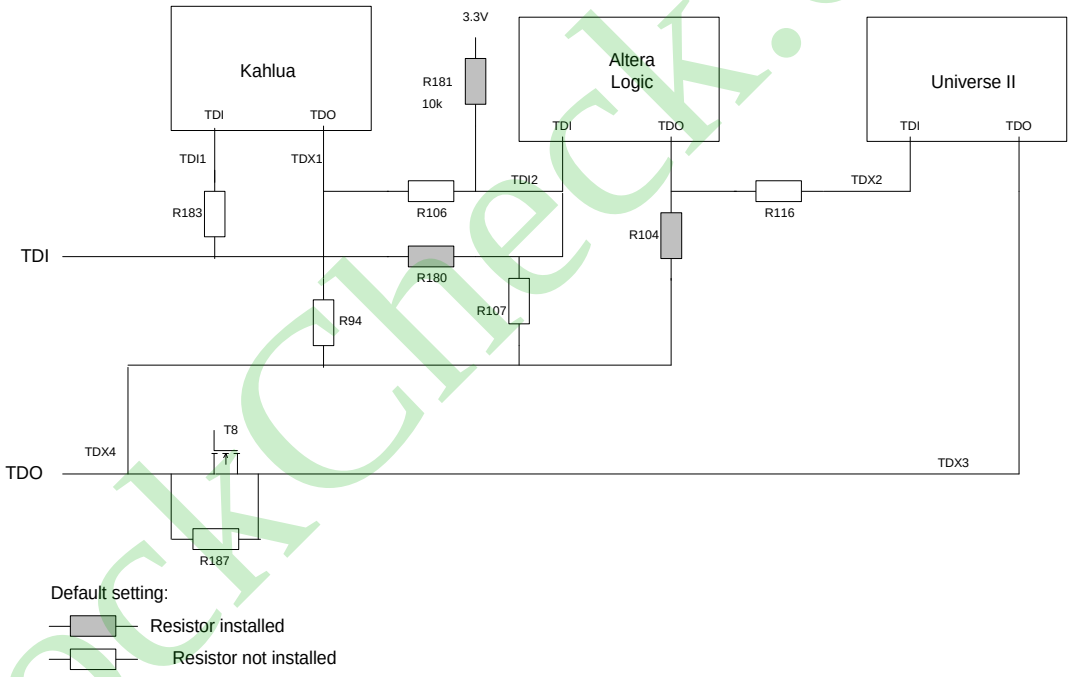
JTAG Subsystem

Description

All the JTAG capable devices on the VMP1 can be accessed through the onboard JTAG chain. The factory setting of the chain is such that only the onboard logic is in the chain. If it is required to access the Processor via the JTAG chain a different setting must be used (some resistors must be reset).

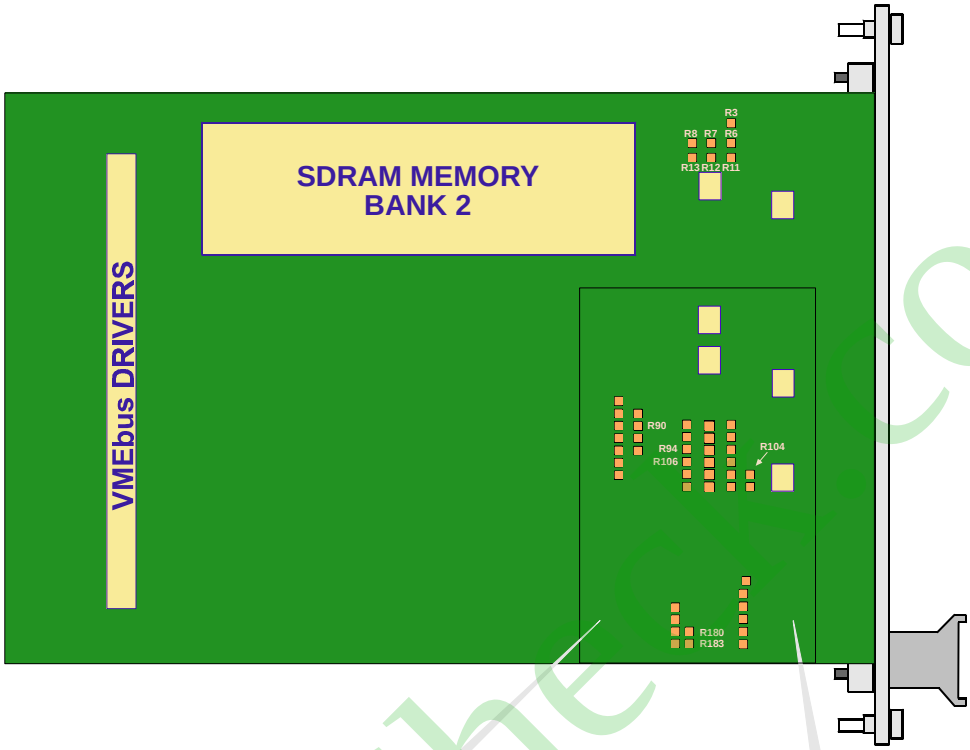
The following picture illustrates the construction of the JTAG chain.

Figure D-1: JTAG Chain Illustration

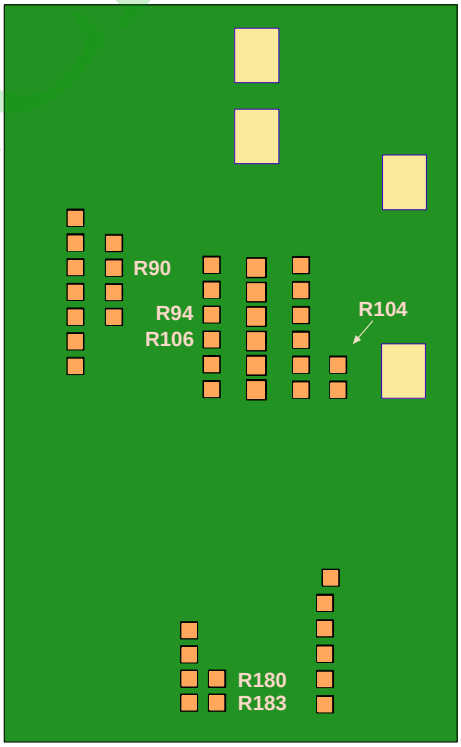


If EMULATOR access to the MPC8240 is required it must be ensured that R94 and R183 are set and also that R104 and R180 are removed (all resistors are 0R).

Figure D-2: Resistor Positions on Reverse of VMP1 Board



MAGNIFIED SECTION



Resistors relevant to the JTAG Subsystem appear on the magnified section of the board

Please note that this diagram is not to scale with other board diagrams